Micron 7400 SSD Series (PCIe® Gen4)

M.2 - 2280: MTFDKBA480TDZ - MTFDKBA960TDZ
M.2 - 22110: MTFDKBG960TDZ - MTFDKBG3T8TDZ
U.3 - 15mm: MTFDKCC800TFC - MTFDKCC7T6TDZ
U.3 - 7mm: MTFDKCB800TFC - MTFDKCB7T6TDZ
E1.S - 25mm: MTFDKBU1T9TDZ - MTFDKBU3T8TDZ
E1.S - 15mm: MTFDKCE960TFC - MTFDKCE3T8TDZ
E1.S - 5.9mm: MTFDKBZ960TFC - MTFDKBZ3T8TDZ

Features

- Micron® 3D TLC NAND Flash
- PCI Express Gen4
  - M.2 single port (x4)
  - U.3 single port (x4)
  - EDSFF E1.S single port (x4)
- NVM Express 1.4
  - Number of name spaces supported: 128
  - Weighted round robin with urgent arbitration supported
  - NVMe subsystem reset supported
  - Interrupt coalescing
  - Number of I/O queue pairs: 128 SQ/CQ
  - Number of admin queue pairs: 1 SQ/CQ
- TCG Storage Security Subsystem Class: Opal Rev 2.01
- Capacity (unformatted)
  - 7400 PRO M.2 2280: 480GB, 960GB
  - 7400 PRO M.2 22110: 960GB, 1920GB, 3840GB
  - 7400 PRO U.3: 960GB, 1920GB, 3840GB, 7680GB
  - 7400 PRO E1.S: 960GB, 1920GB, 3840GB
  - 7400 MAX M.2 2280: 400GB, 800GB
  - 7400 MAX M.2 22110: 800GB, 1600GB, 3200GB
  - 7400 MAX U.3: 800GB, 1600GB, 3200GB, 6400GB
  - 7400 MAX E1.S: 800GB, 1600GB, 3200GB
- Endurance: Total bytes written (TBW)
  - 400GB: Up to 2,190TB
  - 480GB: Up to 8,76TB
  - 800GB: Up to 4,380TB
  - 960GB: Up to 1,752TB
  - 1600GB: Up to 8,760TB
  - 1920GB: Up to 3,504TB
  - 3200GB: Up to 17,520TB
  - 3840GB: Up to 7,008TB
  - 6400GB: Up to 35,040TB
  - 7680GB: Up to 14,016TB
- Enterprise sector size support = 512 and 4096-byte sector size (configurable)
- Security: Digitally signed firmware
- Surprise insertion/surprise removal (SISR) and hot-plug capable
- Self-monitoring, analysis, and reporting technology (SMART)
- Performance[1]
  - Sequential 128KB READ: Up to 6600 MB/s
  - Sequential 128KB WRITE: Up to 5400 MB/s
  - Random 4KB READ: Up to 925,000 IOPS
  - Random 4KB WRITE: Up to 370,000 IOPS
- Latency[2, 3]
  - READ (TYP): 71µs
  - WRITE (TYP): 25µs
- Reliability
  - MTTF: 2 million device hours[4]
  - Static and dynamic wear leveling
  - Uncorrectable bit error rate (UBER): <1 sector per 10^{17} bits read
  - End-to-end data protection
  - Full power-loss protection
- Non-operating shock: 1500G @ 0.5ms
- Non-operating vibration: 20 G_{RMS} 5–3000Hz
- Operating temperature[5]
  - Commercial (0°C to +70°C)
- Field upgradeable firmware
- Operating systems supported natively
  - OpenSUSE 12.3, 13.2
  - Microsoft Windows Server® 2016, 2019
  - Ubuntu® 18.04+
  - CentOS® 7.5+
  - Linux - SUSE Enterprise, Ubuntu
  - VMWare ESXi 6.7+ vSAN 7.0
  - Citrix Xen
  - RHEL® 7.5+, 8.0+
  - UEFI 2.3.1+

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‡Products and specifications discussed herein are for evaluation and reference purposes only and are subject to change by Micron without notice. Products are only warranted by Micron to meet Micron's production data sheet specifications.

- Form factor
  - U.3: 100.45 x 70.10 x 7.00mm
  - U.3: 100.45 x 70.10 x 15.00mm
  - EDSFF E1.S: 31.5 x 111.49 x 5.9mm
  - EDSFF E1.S: 31.5 x 111.49 x 15mm
  - EDSFF E1.S: 31.5 x 111.49 x 25mm
  - M.2: 22.00 x 80.00mm
  - M.2: 22.00 x 110.00mm
- Electrical specification
  - U.3/E1.S power supply: 12V ±8%
  - U.3/E1.S AUX supply: 3.3V ±5%
  - M.2 power supply: 3.3V ±5%

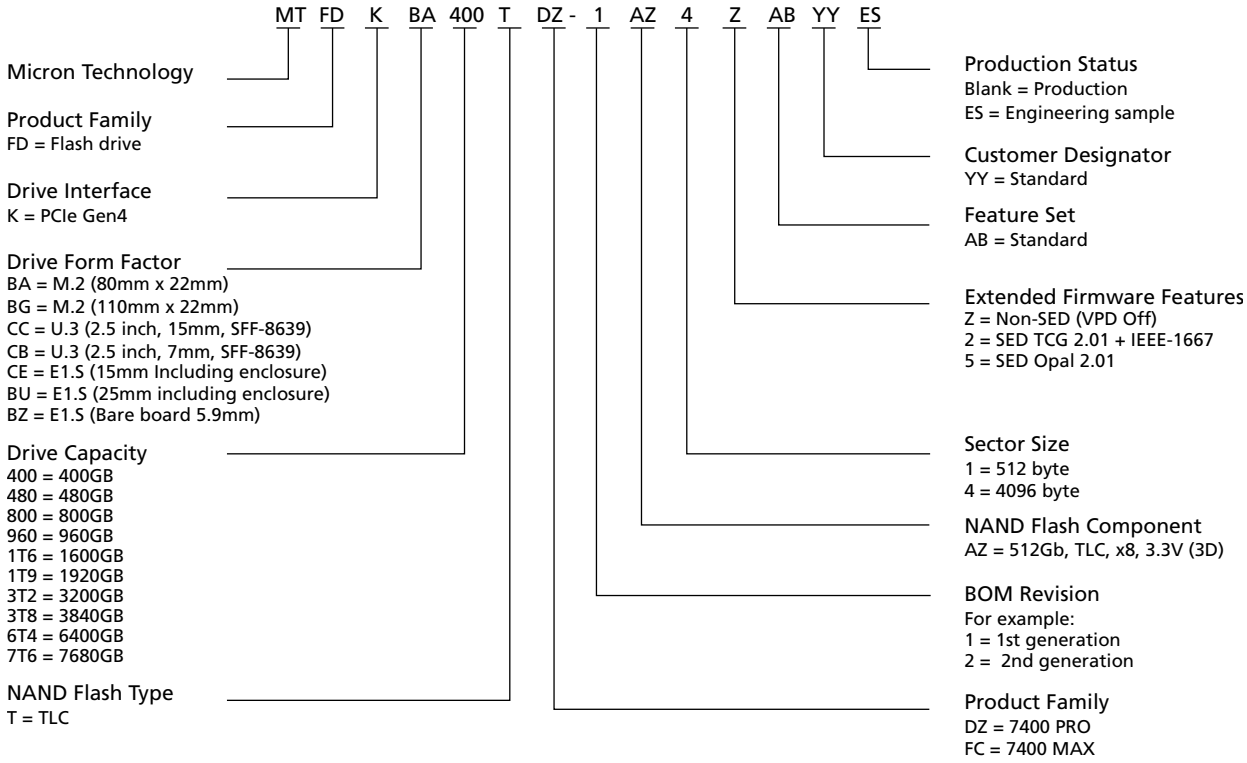
Notes: 1. Steady state as defined by SNIA Solid State Storage Performance Test Specification Enterprise v1.1.
2. 4KB, queue depth 1 transfers used for READ/WRITE latency values.
3. TYP: Median, 50th percentile
4. Product achieves MTTF based on population statistics not relevant to individual units.
5. Temperature measured by SMART.

Warranty: Contact your Micron sales representative for further information regarding the product, including product warranties.

Part Numbering Information

Micron 7400 SSDs are available in different configurations and capacities. The chart below is a comprehensive list of options; not all options listed can be combined to define an offered product. Visit www.micron.com for a list of valid part numbers.

Figure 1: Part Number Chart



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Important Notes and Warnings

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General Description

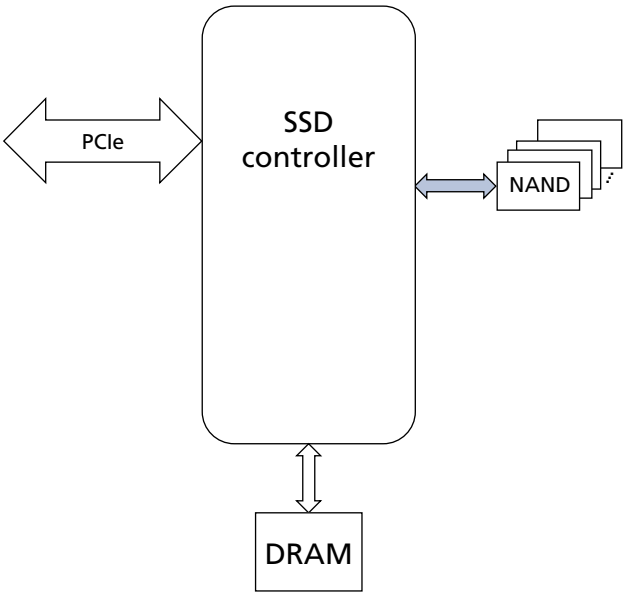
The Micron 7400 SSD Series is a Micron mainstream enterprise/cloud product family. These products use a PCIe Gen4 interface, a non-volatile memory express (NVMe®) protocol, and Micron 3D NAND to provide competitive throughput, IOPS, low latency, and consistent quality of service.

Reliability assurance measures include cyclic redundancy checks (CRC), end-to-end datapath protection, capacitor-backed power loss protection, and Micron extensive validation, quality, and reliability testing. It features thermal monitoring and protection, SMART attributes for status polling, and SMBus for out-of-band management. The Micron 7400 SSD Series offers two endurance classes:

- PRO for read-centric use at roughly 1 DWPD: Available in 480GB (M.2 only), 960GB (M.2, U.3, and E1.S), 1.92TB (M.2, U.3, and E1.S), 3.84TB (M.2, U.3, and E1.S), and 7.68TB (U.3 only) capacities
- MAX for mixed-use workloads at about 3 DWPD: Available in 400GB (M.2 only), 800GB (M.2, U.3, and E1.S), 1.6TB (M.2, U.3, and E1.S), 3.2TB (M.2, U.3, and E1.S), and 6.4TB (U.3 only) capacities.

The self-encrypting drive (SED) adds an AES-256 encryption engine providing hardware-based data encryption, with no loss of SSD performance. The SED follows the TCG/Opal 2.01 specification for trusted peripherals.

Figure 2: Functional Block Diagram



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Performance

Measured performance can vary for a number of reasons. The major factors affecting drive performance are the capacity of the drive and the interface of the host. Additionally, overall system performance can affect the measured drive performance. When comparing drives, it is recommended that all system variables are the same, and only the drive being tested varies.

Performance numbers will vary depending on the host system configuration.

Table 1: Drive Performance – PRO

Parameter	Capacity (GB)										
	M.2 (2280)	M.2 (2280/ 22110)	M.2 (22110)		U.3 (25W/15W)				E1.S (20W/12W)		
Power State 0	480	960	1920	3840	960	1920	3840	7680	960	1920	3840
Sequential (128KB transfer) (MB/s)											
Read	4,400	4,400	4,400	4,400	6,600	6,600	6,600	6,600	6,600	6,600	6,600
Write	530	1,000	2,000	2,200	1,000	2,200	3,500	5400/ 4100	1,000	2,200	3,500
Random (4KB transfer) (IOPS)											
Read	120,000	230,000	420,000	650,000	240,000	430,000	800,000	920,000	240,000	430,000	800,000
Write	21,000	43,000	81,000	100,000	60,000	81,000	125,000	128,000	60,000	81,000	125,000
70/30 random read/ write	45,000	105,000	160,000	200,000	105,000	178,000	275,000	300,000	105,000	178000	275,000
Latency (µs)											
READ (TYP)	85	85	85	85	75	75	75	75	75	75	75
WRITE (TYP)	45	25	15	15	25	15	15	15	25	15	15
READ (99%)	125	120	120	120	110	110	110	110	110	110	110
WRITE (99%)	55	100	125	125	75	65	65	70	75	65	65

Notes: 1. The 7400 M.2 2280 is available in 480GB and 960GB. The 7400 M.2 22110 is available in 960GB, 1920GB, and 3840GB.

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Table 2: Drive Performance – MAX

Parameter Power State 0	Capacity (GB)										
	M.2 (2280)	M.2 (2280/ 22110)	M.2 (22110)		U.3 (25W/15W)				E1.S (20W/12W)		
	400	800	1600	3200	800	1600	3200	6400	800	1600	3200
Sequential (128KB transfer) (MB/s)											
Read	4,400	4,400	4,400	4,400	6,600	6,600	6,600	6,600	6,600	6,600	6,600
Write	530	1,000	2,000	22,00	1,000	2,200	3,500	5,400	1,000	2,200	3,500
Random (4KB transfer) (IOPS)											
Read	120,000	230,000	420,000	650,000	240,000	430,000	800,000	925,000	240,000	430,000	800,000
Write	55,000	118,000	172,000	206,000	124,000	225,000	348,000	370,000	124,000	225,000	348,000
70/30 random read/ write	75,000	153,000	261,000	360,000	160,000	278,000	455,000	610,000	160,000	278,000	455,000
Latency (µs)											
READ (TYP)	85	85	85	85	75	75	75	75	75	75	75
WRITE (TYP)	45	25	15	15	25	15	15	15	25	15	15
READ (99%)	120	120	120	110	110	110	110	110	110	110	110
WRITE (99%)	100	125	125	65	65	65	65	70	75	65	65

Notes: 1. Performance values measured under the following conditions:
- Steady state as defined by SNIA Solid State Storage Performance Test Specification Enterprise v1.1
- Drive write cache enabled
- NVMe power state 0
- Sequential workloads measured using FIO with a queue depth of 32
- Random workloads measured using FIO with a queue depth of 128

2. Performance values measured with the following system configuration:
- Generic X570 Motherboard
- AMD Ryzen 7 3700X 8-Core CPU @ 2.6 GHz
- DDR4 16GB @ 3200 MHz

3. Latency values measured under the following configuration:
- Random workloads using FIO with 4KB transfers and a queue depth of 1
- TYP = median, 50th percentile

4. System variations will affect measured results.

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Logical Block Address Configuration

The drive is set to report the number of logical block addresses (LBA) that will ensure sufficient storage space for the specified capacity. Standard LBA settings, based on the JESD2 18A solid state drive (SSD) requirements and endurance test method, are shown below.

Table 3: Standard LBA Settings

Capacity (GB)	512-Byte Sector LBA Count	4096-Byte Sector LBA Count
400	781,422,768	97,677,846
480	937,703,088	117,212,886
800	1,562,824,368	195,353,046
960	1,875,385,008	234,423,126
1600	3,125,627,568	390,703,466
1920	3,750,748,848	468,843,606
3200	6,251,233,968	781,404,246
3840	7,501,476,528	937,684,566
6400	12,502,446,768	1,562,805,846
7680	15,002,931,888	1,875,366,486

Reliability

The SSD incorporates advanced technology for defect and error management, using various combinations of hardware-based error correction algorithms and firmware-based static and dynamic wear-leveling algorithms.

Over the life of the SSD, uncorrectable errors may occur. An uncorrectable error is defined as data that is reported as successfully programmed to the SSD but when it is read out of the SSD, the data differs from what was programmed.

Table 4: Uncorrectable Bit Error Rate

Uncorrectable Bit Error Rate	Operation
<1 sector per 10^{17} bits read	READ

Mean Time to Failure

Mean time to failure (MTTF) for the SSD can be predicted based on the component reliability data using the methods referenced in the Telcordia SR-332 reliability prediction procedures for electronic equipment.

Table 5: MTTF

Capacity	MTTF (Operating Hours)
All capacities	2 million

Notes: 1. The product achieves a mean time to failure (MTTF) based on population statistics, not relevant to individual units.

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Endurance

SSD endurance is dependent on many factors, including: usage conditions applied to the drive, drive performance and capacity, formatted sector size, error correction codes (ECCs) in use, internal NAND PROGRAM/ERASE cycles, write amplification factor, wear-leveling efficiency of the drive, over-provisioning ratio, valid user data on the drive, drive temperature, NAND process parameters, and data retention time.The device is designed to operate under a wide variety of conditions, while delivering the maximum performance possible and meeting enterprise market demands.

While actual endurance varies depending on conditions, the drive lifetime can be estimated based on capacity, assumed fixed-use models, ECC, and formatted sector size.

Lifetime estimates for the device are shown in the following tables in total bytes written.

Table 6: Total Bytes Written

Model	Capacity (GB)	4K Random Total Bytes Written (TB)	128K Sequential Total Bytes Written (TB)
PRO	480	876	3843
	960	1752	6790
	1920	3504	14,412
	3840	7008	25,760
	7680	14,016	48,871
MAX	400	2190	4185
	800	4380	8095
	1600	8760	16,496
	3200	17,520	31,881
	6400	35,040	62,827

Notes: 1. All values provided are for reference only and are not warrantied values. For warranty information, visit https://www.micron.com/support/sales-support/returns-and-warranties/enterprise-ssd-warranty or contact your Micron sales representative.
2. Values represent the theoretical maximum endurance for the given transfer size and type. Actual lifetime will vary by workload. Refer to Percentage Used in the SMART/Health Information (Log Identifier 02h) to check the device life used.

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Electrical Characteristics

Environmental conditions beyond those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 7: Power Consumption – PRO

Parameter	Capacity (GB)											Unit
	M.2				U.3				E1.S			
Power State 0	480	960	1920	3840	960	1920	3840	7680	960	1920	3840	
Active read (maximum RMS)	7.1	7.1	7.2	7.4	10.0	10.0	10.8	11.8	10.0	10.0	10.8/ 10.6[1]	W
Active write (maximum RMS)	4.2	5.2	7.2	8.1	7.0	8.9	12.8	15.6/ 14.3[1]	7.0	8.9	12.8/ 11.9[1]	W
128K sequential read (average RMS)	7.1	7.1	7.2	7.3	10.0	10.0	10.6	11.8	10.0	10.0	10.6/ 10.4[1]	W
128K sequential write (average RMS)	4.2	5.2	7.2	7.9	6.9	8.8	11.3	15.5/ 14.1[1]	6.9	8.7	11.3/ 10.9[1]	W
4K random read (average RMS)	3.8	4.3	4.9	5.1	6.0	6.3	6.3	6.3	6.0	6.3	6.9/ 6.7[1]	W
4K random write (average RMS)	4.4	5.6	6.7	7.2	7.0	9.0	10.9	12.6	7.0	9.0	10.9	W
Idle (average RMS)	3.0	3.0	3.0	3.0	4.8	4.8	4.8	4.8	5.4	4.8	4.8	W

Notes: 1. Split indicates 7mm/15mm.

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Table 8: Power Consumption – MAX

Parameter Power State 0	Capacity (GB)											Unit
	M.2				U.3				E1.S			
	400	800	1600	3200	800	1600	3200	6400	800	1600	3200	
Active read (maximum RMS)	7.1	7.1	7.2	7.4	10.0	10.0	10.8	11.8	10.0	10.0	10.8/ 10.6[1]	W
Active write (maximum RMS)	4.2	5.2	7.2	8.1	7.0	8.9	12.8	15.6/ 14.3[1]	7.0	8.9	12.8/ 11.9[1]	W
128K sequential read (average RMS)	7.1	7.1	7.2	7.3	10.0	10.0	10.6	11.8	10.0	10.0	10.6/ 10.4[1]	W
128K sequential write (average RMS)	4.2	5.2	7.2	7.9	6.9	8.8	11.3	15.5/ 14.1[1]	6.9	8.7	11.3/ 10.9[1]	W
4K random read (average RMS)	3.8	4.3	4.9	5.1	6.0	6.3	6.3	6.3	6.0	6.3	6.9/ 6.7[1]	W
4K random write (average RMS)	4.4	5.6	6.7	7.2	7.0	9.0	10.9	12.6	7.0	9.0	10.9	W
Idle (average RMS)	3.0	3.0	3.0	3.0	4.8	4.8	4.8	5.4	4.8	4.8	4.8	W

Notes: 1. Split indicates 7mm/15mm.
2. Power limiting is configured through Set/Get Features Power Management.
3. Power consumption measurements are for reference only; actual workload power consumption will vary.

Table 9: Operating Voltage – U.3 and EDSFF

Power Rail	Electrical Parameter	Value
12V	Operating voltage	12 Vdc (±8%)
	MIN/MAX rise time	10ms/100ms
	Fall time	<5s
	MIN power-off time	50ms
	Inrush current (typical peak)	2.0A
	MAX average current (RMS)	1.2A
3.3 V_{AUX}	Operating voltage	3.3 Vdc
	MIN/MAX rise time	1ms/50ms
	MIN/MAX fall time	1ms/5s
	MAX average current	20mA

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Table 10: Operating Voltage – M.2

Power Rail	Electrical Parameter	Value
3.3V	Operating voltage	3.3Vdc (±5%)
	MIN/MAX rise time	1ms/50ms
	MIN/MAX fall time	1ms/5s
	MIN power-off time	1s
	Inrush current (typical peak)	2.5A
	MAX average current (RMS)	2.4A

Table 11: Temperature and Airflow

Temperature and Airflow	Specification	Notes
Operating temperature (as indicated by the SMART temperature attribute)	0°C to 70°C	1
Operating ambient temperature	0°C to 35°C	2
Operating airflow	See Table 12	3
Storage temperature	–40°C to 85°C	
Rate of temperature change	20°C/hr	
Relative humidity (non condensing)	5% to 90%	

Notes: 1. If SMART temperature exceeds 77°C, performance will be throttled.
2. Temperature of air impinging on the drive.
3. Airflow must flow along the length of the drive and is measured upstream.

Table 12: Airflow Measurements

Device	Specification
M.2 Gen3 2280	1.5 m/s
M.2 Gen3 22110	1.5 m/s
M.2 Gen4 2280	2.5 m/s
M.2 Gen4 22110	2.5 m/s
E1.S 5.9mm	1.41 CFM (rack spacing cross-section; 35mm x 9mm)
E1.S 15mm	1.5 CFM (rack spacing cross-section; 35mm x 16mm)
E1.S 25mm	4.1 CFM (rack spacing cross-section; 35mm x 26mm)
U.3 7mm	1.5 m/s
U.3 15mm	1.5 m/s

Table 13: Shock and Vibration

Parameter/Condition	Specification
Non-operating shock	1500G @ 0.5ms half-sine
Non-operating vibration	20 G_{RMS} 5–3000Hz

Notes: 1. Shock and vibration ratings refer to the ability to withstand stress events only. Prolonged or repeated exposure to conditions listed or greater stresses may result in permanent damage to the device. Functional operation of the device under these conditions is not implied. See warranty for more information.

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Data Retention

Data retention refers to the capability of the SSD media (that is, NAND flash) to retain programmed data. The three primary factors that affect data retention are:

- Power-on/power-off state: Data retention generally improves when the SSD is in use (that is, not shelved in a power-off state).
- Temperature: Data retention decreases as the temperature increases.
- Number of PROGRAM/ERASE cycles on the media: When the SSD ships from the factory, it is typically able to retain user data for up to 5 years in a powered-off state.

Data retention is guaranteed for three months at 40ºC (MAX), which assumes worst-case power and media wear (the SSD remains in a powered-off state and has reached end of life).

Wear Leveling

The Micron 7400 SSD Series uses sophisticated wear-leveling algorithms to maximize endurance by distributing PROGRAM/ERASE cycles uniformly across all blocks in the array. Both static and dynamic wear leveling are utilized to optimize the drive's lifespan. Both types of wear leveling aim to distribute "hot" data away from blocks that have experienced relatively heavy wear. Static wear leveling accomplishes this by moving data that has not been modified for an extended period of time out of blocks that have seen few PROGRAM/ERASE cycles and into more heavily worn blocks. This frees up fresher blocks for new data while reducing expected wear on tired blocks. Dynamic wear leveling, by contrast, acts on in-flight data to ensure it is preferentially written to the least worn free blocks rather than those closer to the end of their rated life. These techniques are used together within the controller to optimally balance the wear profile of the NAND array.

Firmware Update Capability

The Micron 7400 SSD Series supports firmware updates as defined by the NVMe specification. When a FIRMWARE DOWNLOAD command completes, a FIRMWARE COMMIT command must be issued. Firmware activation is supported without a controller reset.

Power-Loss Subsystem and Rebuild

The Micron 7400 SSD Series supports an unexpected power loss with a power-backed write cache. No user data is lost during an unexpected power loss. When power is subsequently restored, the SSD returns to a ready state within a maximum of 120 seconds.

Boot

The Micron 7400 SSD Series supports UEFI boot.

Management Component Transport Protocol

The Micron 7400 SSD Series supports Management Component Transport Protocol (MCTP) over SMBus/PCIe across all form factors to provide management information from endpoint to endpoint. Refer to NVMe-MI specification Rev 1.1 for details.

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Identify – Identify Controller Data Structure

Table 14: Identify – Identify Controller Data Structure

Bytes	Default Value	Description
01:00	1344h	**PCI Vendor ID (VID):** Contains the Micron identifier assigned by the PCI SIG.
03:02	1344h	**PCI Subsystem Vendor ID (SSVID):** Contains the Micron identifier assigned by the PCI SIG for the subsystem.
23:04	Variable	**Serial Number (SN):** Contains the serial number for the NVM subsystem as an ASCII string.
63:24	Variable	**Model Number (MN):** Contains the model number for the NVM subsystem as an ASCII string.
71:64	Variable	**Firmware Revision (FR):** Contains the currently active firmware revision for the NVM subsystem.
72	3	**Recommended Arbitration Burst (RAB):** This is the recommended arbitration burst size.
75:73	00A075h	**IEEE OUI Identifier (IEEE):** Contains the organization unique identifier (OUI).
76	0	**Controller Multi-Path I/O and Namespace Sharing Capabilities (CMIC):** This field specifies multi-path I/O and namespace sharing capabilities of the controller and NVM subsystem. Bits 7:3: Reserved. Bit 2 = 0: The controller is associated with a PCI function. Bit 1 = 0: The NVM subsystem contains only a single controller. Bit 0 = 0: The NVM subsystem contains only a single PCI Express port.
77	10	**Maximum Data Transfer Size (MDTS):** This field indicates the maximum data transfer size between the host and the controller. The host should not submit a command that exceeds this transfer size. If a command is submitted that exceeds the transfer size, then the command is aborted with a status of Invalid Field in command. The value is in units of the minimum memory page size (4096 bytes) and is reported as a power of two (2^n).
79:78	01h	**Controller ID (CNTLID):** Contains the NVM subsystem unique controller identifier associated with the controller.
83:80	10400h	**Version (VER):** This register indicates the major and minor version of the NVM Express specification that the controller implementation supports.
87:84	0	**RTD3 Resume Latency (RTD3R):** This field indicates the typical latency in microseconds resuming from Runtime D3 (RTD3).
91:88	0	**RTD3 Entry Latency (RTD3E):** This field indicates the typical latency in microseconds to enter Runtime D3 (RTD3).

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Table 14: Identify – Identify Controller Data Structure

Bytes	Default Value	Description
95:92	300h	**Optional Asynchronous Events Supported (OAES):**This field indicates the optional asynchronous events supported by the controller. A controller shall not send optional asynchronous events before they are enabled by host software. Bits 31:15: Reserved. Bit 14 = 0: The controller does not support the Endurance Group Event Aggregate Log Page Change Notices event. Bit 13 = 0: The controller does not support the LBA Status Information Notices event. Bit 12 = 0: The controller does not support the Predictable Latency Event Aggregate Log Change Notices event. Bit 11 = 0: The controller does not support the Asymmetric Namespace Access Change Notices event. Bit 10: Reserved. Bit 9 = 1: Indicates the controller supports the Firmware Activation Notices event. Bit 8 = 1: Indicates the controller supports sending the Namespace Attribute Changed event. Bits 7:0: Reserved.
99:96	0	**Controller Attributes (CTRATT):** This field indicates attributes of the controller. Bits 31:10: Reserved. **UUID List** Bit 9 = 0: The controller does not support reporting of a UUID List. **SQ Associations** Bit 8 = 0: The controller does not support SQ associations. **Namespace Granularity** Bit 7 = 0: The controller does not support reporting of Namespace Granularity. **Traffic Based Keep Alive Support - TBKAS** Bit 6 = 0: The controller supports restarting the Keep Alive Timer only if a Keep Alive command is processed during the Keep Alive Timeout Interval. **Predictable Latency Mode** Bit 5 = 0: The controller does not support Predictable Latency Mode. **Endurance Groups** Bit 4 = 0: The controller does not support Endurance Groups. **Read Recovery Levels** Bit 3 = 0: The controller does not support Read Recovery Levels. **NVM Sets** Bit 2 = 0: The controller does not support NVM sets. Bit 1 = 0: The controller does not support host control of whether the controller may exceed the power of a non-operational state for the purpose of executing controller initiated background operations in a non-operational state (that is, Non-Operational Power State Permissive Mode not supported). Bit 0 = 0: The controller does not support a 128-bit Host Identifier.
101:100	0h	**Read Recovery Levels Supported (RRLS):** Bit 0 = 0: The corresponding Read Recovery Level is not supported.
110:102	–	Reserved
111	1h	**Controller Type (CNTRLTYPE):** Byte 1 = 1h: Indicates I/O controller

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Table 14: Identify – Identify Controller Data Structure

Bytes	Default Value	Description
127:112	0	**FRU Globally Unique Identifier (FGUID):** Contains a 128-bit value that is globally unique for a given Field Replaceable Unit (FRU). Refer to the NVM Express Management Interface (NVMe-MI) specification for the definition of a FRU. This field remains fixed throughout the life of the FRU. This field shall contain the same value for each controller associated with a given FRU. This field uses the EUI-64 based 16-byte designator format. Bytes 122:120 contain the 24-bit Organizationally Unique Identifier (OUI) value assigned by the IEEE Registration Authority. Bytes 127:123 contain an extension identifier assigned by the corresponding organization. Bytes 119:112 contain the vendor specific extension identifier assigned by the corresponding organization. See the IEEE EUI-64 guidelines for more information. This field is big endian (refer to section 7.10). When not implemented, this field contains a value of 0h.
129:128	0000h	**Command Retry Delay Time 1 (CRDT1):** If the Do Not Retry (DNR) bit is cleared to 0 in the CQE and the Command Retry Delay (CRD) field is set to 01b in the CQE, then this value indicates the command retry delay time in units of 100ms.
131:130	0000h	**Command Retry Delay Time 2 (CRDT2):** If the DNR bit is cleared to 0 in the CQE and the CRD field is set to 10b in the CQE, then this value indicates the command retry delay time in units of 100ms.
133:132	0000h	**Command Retry Delay Time 3 (CRDT3):** If the DNR bit is cleared to 0 in the CQE and the CRD field is set to 11b in the CQE, then this value indicates the command retry delay time in units of 100ms.
139:134	–	Reserved
255:240	03000000000000000000000000000000h	**NVMe Management Interface:**NVMe Management Interface is supported.
257:256	0000000010111 11b	**Optional Admin Command Support (OACS):** This field indicates the optional Admin commands supported by the controller. Bits 15:10: Reserved. Bit 9 = 0: The controller does not support the Get LBA Status capability. Bit 8 = 0: The controller does not support the DOORBELL BUFFER CONFIG command. Bit 7 = 0: The controller does not support the VIRTUALIZATION MANAGEMENT command. Bit 6 = 1: The controller supports the NVMe-MI SEND and NVMe-MI RECEIVE commands. Bit 5 = 0: The controller does not support Directives. Bit 4 = 1: The controller supports the Device Self Test command. Bit 3 = 1: The controller supports the NAMESPACE MANAGEMENT and NAMESPACE ATTACHMENT commands. Bit 2 = 1: The controller supports the FIRMWARE COMMIT and FIRMWARE IMAGE DOWNLOAD commands. Bit 1 = 1: The controller supports the FORMAT NVM command. Bit 0 = 1: The controller supports the SECURITY SEND and SECURITY RECEIVE commands.
258	3h	**Abort Command Limit (ACL):** This field is used to convey the maximum number of concurrently outstanding ABORT commands supported by the controller.
259	7h	**Asynchronous Event Request Limit (AERL):** This field is used to convey the maximum number of concurrently outstanding ASYNCHRONOUS EVENT REQUEST commands supported by the controller.

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Table 14: Identify – Identify Controller Data Structure

Bytes	Default Value	Description
260	00010111b	**Firmware Updates (FRMW):** This field indicates capabilities regarding firmware updates. Bits 7:5: Reserved. Bit 4 = 1: The controller supports firmware activation without a reset. Bits 3:1 = 011: The number of firmware slots that the controller supports. Bit 0 = 1: The first firmware slot (slot 1) is read only. Note: The addition of the AWOR feature is planned for a future firmware update.
261	00011110b	**Log Page Attributes (LPA):** This field indicates optional attributes for log pages that are accessed via the GET LOG PAGE command. Bits 7:5: Reserved Bit 4 = 1: The controller supports the Persistent Event log. Bit 3 = 1: The controller supports the Telemetry Host-Initiated and Telemetry Controller-Initiated log pages and sending Telemetry Log Notices. Bit 2 = 1: The controller supports extended data for the Get Log Page. Bit 1 = 1: The controller supports the Command Effects Log Page. Bit 0 = 0: The controller does not support the SMART/Health Information Log Page on a per namespace basis.
262	FFh	**Error Log Page Entries (ELPE):** This field indicates the number of Error Information log entries that are stored by the controller. This field is a 0's based value.
263	4	**Number of Power States Support (NPSS):** This field indicates the number of NVM Express power states supported by the controller. This is a 0's based value.
264	1	**Admin Vendor-Specific Command Configuration (AVSCC):** All Admin Vendor-Specific Commands use the command format defined in NVMe 1.4.
265	0	**Autonomous Power State Transition Attributes (APSTA):** This field indicates the attributes of the autonomous power state transition feature. Bits 7:1: Reserved. Bit 0 = 0: The controller does not support autonomous power state transitions.
267:266	15Eh	**Warning Composite Temperature Threshold (WCTEMP):** This field indicates the minimum Composite Temperature field value (Temperature value reported in the SMART/Health Information log) that indicates an overheating condition during which controller operation continues. Immediate remediation is recommended (for example, additional cooling or workload reduction). The platform should strive to maintain a composite temperature below this value.
269:268	166h	**Critical Composite Temperature Threshold (CCTEMP):** This field indicates the minimum Composite Temperature field value (Temperature value reported in the SMART/Health Information log) that indicates a critical overheating condition (for example, automatic device shutdown).
271:270	14h	**Maximum Time for Firmware Activation (MTFA):** The maximum time the controller temporarily stops processing commands to activate the firmware image (in 100ms).
275:272	0	**Host Memory Buffer Preferred Size (HMPRE):** Host Memory Buffer Preferred Size is not supported.
279:276	0	**Host Memory Buffer Minimum Size (HMMIN):** Host Memory Buffer Minimum Size is not supported.
295:280	Variable	**Total NVM Capacity (TNVMCAP):** This field indicates the total NVM capacity in the NVM subsystem. The value is in bytes.
311:296	Variable	**Unallocated NVM Capacity (UNVMCAP):** This field indicates the unallocated NVM capacity in the NVM subsystem. The value is in bytes.

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Table 14: Identify – Identify Controller Data Structure

Bytes	Default Value	Description
315:312	0	**Replay Protected Memory Block Support (RPMBS):** Replay Protected Memory Blocks is not supported. **Access Size:** The maximum number of 512 bytes units of data that may be read or written per RPMB access by SECURITY SEND or SECURITY RECEIVE commands for this controller. Bits 31:24 = 0: Then ignore this field. **Total Size:** The number of 128KB units of data in each RPMB supported in the controller. Bits 23:16 = 0: Then ignore this field. Bits 15:6: Reserved. **Authentication Method:** The authentication method used to access all RPMB. Bits 5:3 = 000b: HMAC SHA-256 is used. **Number of RPMB Units:** The controller does not support Replay Protected Memory Blocks.
317:316	2	**Extended Device Self-test Time (EDSTT):** When the DEVICE SELF-TEST command is supported, then this field indicates the nominal amount of time in one minute units that the controller takes to complete an EXTENDED DEVICE SELF-TEST operation when in power state 0. When the DEVICE SELF-TEST command is not supported, then this field is reserved.
318	1	**Device Self-test Options (DSTO):** Indicates the optional DEVICE SELF-TEST command or operation behaviors supported by the controller or NVM subsystem. Bits 7:1: Reserved Bit 0 = 1: NVM subsystem supports only one DEVICE SELF-TEST operation in progress at a time.
319	0	**Firmware Update Granularity (FWUG):** Indicates the minimum granularity and alignment of the data provided in the FIRMWARE IMAGE DOWNLOAD command. When the data in the FIRMWARE IMAGE DOWNLOAD command does not conform to these granularity and alignment requirements, the firmware update may fail. The value is reported in 4KB units.
321:320	0	**Keep Alive Support (KAS):** This field indicates attributes for SANITIZE operations.
323:322	1	**Host Controlled Thermal Management Attributes (HCTMA):** Bit 0 = 1: The controller supports host controller thermal management.
325:324	15Eh	**Minimum Thermal Management Temperature (MNTMT):** Minimum Thermal Management Temperature reports in degrees Kelvin.
327:326	166h	**Maximum Thermal Management Temperature (MXTMT):** Maximum Thermal Management Temperature reports in degrees Kelvin.
331:328	A0000003h	**Sanitize Capabilities (SANICAP):** Sanitize Capabilities is not supported. **No-Deallocate Modifies Media After Sanitize (NODMMAS):** Bits 31:30 = 10b: Media is additionally modified by the NVMe controller after SANITIZE operation completes successfully. The SANITIZE operation completed event does not occur until the additional media modification associated with this field has completed. **No-Deallocate Inhibited (NDI):** Refer to NVMe Spec 1.4 for detail. **Overwrite Support (OWS):** Bit 2 = 0: The controller does not support the OVERWRITE SANITIZE operation. **Block Erase Support (BES):** Bit 1 = 1: The controller supports the BLOCK ERASE SANITIZE operation. **Crypto Erase Support (CES):** Bit 0 = 1: The controller supports the CRYPTO ERASE SANITIZE operation.

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Table 14: Identify – Identify Controller Data Structure

Bytes	Default Value	Description
335:332	0	**Host Memory Buffer Minimum Descriptor Entry Size (HMMINDS):** This field indicates the minimum usable size of a Host Memory Buffer Descriptor Entry in 4KB units.
337:336	0	**Host Memory Maximum Descriptors Entries (HMMAXD):** This field indicates the number of usable Host Memory Buffer Descriptor Entries.
339:338	0	**NVM Set Identifier Maximum (NSETIDMAX):** This field defines the maximum value of a valid NVM set Identifier for any controller in the NVM subsystem.
341:340	0	**Endurance Group Identifier Maximum (ENDGIDMAX):** This field defines the maximum value of a valid Endurance Group Identifier for any controller in NVM subsystem.
342	0	**ANA Transition Time (ANATT):** This field indicates the maximum amount of time, in seconds, for a transition between ANA states or the maximum amount of time, that the controller reports the ANA change state.
343	0	**Asymmetric Namespace Access Capabilities (ANACAP):** The controller does not support this feature.
347:344	0	**ANA Group Identifier Maximum (ANAGRPMAX):** The controller does not support Asymmetric Namespace Access Reporting.
351:348	0	**Number of ANA Group Identifiers (NANAGRPID):** The controller does not support Asymmetric Namespace Access Reporting.
355:352	0x200	**Persistent Event Log Size (PELS):** This field indicates the minimum reportable size for the Persistent Event Log.
511:356	–	Reserved
512	66h	**Submission Queue Entry Size (SQES):** This field defines the required and maximum submission queue entry size when using the NVM command set. Bits 7:4 = 6h: Defines the maximum submission queue entry size when using the NVM command set. The value is in bytes and is reported as a power of two (2^n). Bits 3:0 = 6h: Defines the required submission queue entry size when using the NVM command set. The value is in bytes and is reported as a power of two (2^n).
513	44h	**Completion Queue Entry Size (CQES):** This field defines the required and maximum completion queue entry size when using the NVM command set. Bits 7:4 = 4h: Defines the maximum completion queue entry size when using the NVM command set. The value is in bytes and is reported as a power of two (2^n). Bits 3:0 = 4h: Defines the required completion queue entry size when using the NVM command set. The value is in bytes and is reported as a power of two (2^n).
515:514	0	**Maximum Outstanding Commands (MAXCMD):** Maximum Outstanding Commands is not supported.
519:516	80h	**Number of Namespaces (NN):** This field defines the number of valid namespaces present for the controller.

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Table 14: Identify – Identify Controller Data Structure

Bytes	Default Value	Description
521:520	5Fh	**Optional NVM Command Support (ONCS):** Indicates the optional NVM commands and features supported by the controller. Bits 15:8: Reserved. Bit 7 = 0: The controller does not support the VERIFY command. Bit 6 = 1: The controller supports the Timestamp feature. Bit 5 = 0: The controller does not support reservations. Bit 4 = 1: The controller supports the save field in the SET FEATURES command and the select field in the GET FEATURES command. Bit 3 = 1: The controller supports the WRITE ZEROS command. Bit 2 = 1: The controller supports the DATASET MANAGEMENT command. Bit 1 = 1: The controller supports the WRITE UNCORRECTABLE command. Bit 0 = 1: The controller supports the COMPARE command.
523:522	1	**Fused Operation Support (FUSES):** This field indicates the fused operations that the controller supports. Bits 15:1: Reserved. Bit 0 = 1: The controller supports the compare and write fused operation
524	4h	**Format NVM Attributes (FNA):** This field indicates attributes for the FORMAT NVM command. Bit 2 = 1: Cryptographic erase is supported. Bit 1 = 0: Any secure erase performed as part of a format operation results in a secure erase of all namespaces in the NVM subsystem. Bit 0 = 0: The controller supports format on a per namespace basis
525	0110b	**Volatile Write Cache (VWC):** This field indicates attributes related to the presence of a volatile write cache in the implementation. Bits 7:3: Reserved. Bits 2:1 = 11b: The Flush command supports the NSID field set to FFFFFFFFh. Bit 0 = 0: A volatile write cache is not present.
527:526	1Fh	**Atomic Write Unit Normal (AWUN):** The size 64KB of the WRITE operation guaranteed to be written atomically to the NVM across all namespaces with any supported namespace format during normal operation. If a specific namespace guarantees a larger size than is reported in this field, then this namespace specific size is reported in the NAWUN field in the Identify Namespace data structure. If a WRITE command is submitted with size less than or equal to the AWUN value, the host is guaranteed that the WRITE command is atomic to the NVM with respect to other READ or WRITE commands. If a WRITE command is submitted with size greater than the AWUN value, then there is no guarantee of command atomicity. AWUN does not have any applicability to write errors caused by power failure (refer to Atomic Write Unit Power Fail).
529:528	1Fh	**Atomic Write Unit Power Fail (AWUPF):** The size 64KB of the WRITE operation guaranteed to be written atomically to the NVM across all namespaces with any supported namespace format during a power fail or error condition. If a specific namespace guarantees a larger size than is reported in this field, then this namespace specific size is reported in the NAWUPF field in the Identify Namespace data structure. The AWUPF value shall be less than or equal to the AWUN value. If a WRITE command is submitted with size less than or equal to the AWUPF value, the host is guaranteed that the write is atomic to the NVM with respect to other WRITE or WRITE commands. If a WRITE command is submitted that is greater than this size, there is no guarantee of command atomicity. If the write size is less than or equal to the AWUPF value and the WRITE command fails, then subsequent READ commands for the associated logical blocks shall return data from the previous successful WRITE command. If a WRITE command is submitted with size greater than the AWUPF value, then there is no guarantee of data returned on subsequent reads of the associated logical blocks.

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Table 14: Identify – Identify Controller Data Structure

Bytes	Default Value	Description
530	1	**NVM Vendor-Specific Command Configuration (NVSCC):** Bits 7:1: Reserved. Bit 0 = 1: All NVM Vendor-Specific Commands use the command format defined in NVMe 1.4.
531	0	**Name Write Protection Capabilities (NWPC):** This field indicates the optional name-space write protection capabilities supported by the controller. Bits 7:3: Reserved. Bit 2 = 0: The controller does not support the Permanent Write Protect state. Bit 1 = 0: The controller does not support Write Protect Until Power Cycle state. Bit 0 = 0: The controller does not support Namespace Write Protection and bits 2:1 shall be cleared to 00b.
533:532	1Fh	**Atomic Compare & Write Unit (ACWU):** The size 64KB of the WRITE operation guaran-teed to be written atomically to the NVM across all namespaces with any supported namespace format for a COMPARE and WRITE fused operation.
535:534	0	Reserved.
539:536	0	**SGL Support (SGLS):** Bits 31:22: Reserved. Bit 21 = 0: The controller does not support the Transport SGL Data Block descriptor. Bit 20 = 0: The address field specifying an offset is not supported. Bit 19 = 0: Use of a MPTR containing an SGL Descriptor is not supported. Bit 18 = 0: The SGL length shall be equal to the amount of data to be transferred. Bit 17 = 0: Use of a bye aligned contiguous physical buffer of metadata is not supported. Bit 16 = 0: The SGL Bit Bucket descriptor is not supported. Bits 15:3: Reserved. Bit 2 = 0: The controller does not support the Keyed SGL Data Block descriptor. Bits 1:0 = 00b: SGLs are not supported.
543:540	128	This field indicates the maximum number of namespaces supported by the NVM subsys-tem. If the controller supports Asymmetric Namespace Access Reporting, then this field shall be set to a non-zero value that is less than or equal to the NN value.
767:544	–	Reserved
1023:768	Variable	**NVM Subsystem NVMe Qualified Name (SUBNQN):** Specifies the NVM Subsystem NVMe Qualified Name as a UTF-8 null-terminated string. Refer to section 7.9 for the defi-nition of NVMe Qualified Name.
2047:1024	–	Reserved.
2079:2048	U.3 = 9C4h M.2 = 339h E1.S = 4B0h	**Power State 0 Descriptor (PSD0):** This field indicates the characteristics of power state 0. The format of this field is defined in .
2111:2080	U.3 = 76Ch M.2 = 2BCh E1.S = 384h	**Power State 1 Descriptor (PSD1):** This field indicates the characteristics of power state 1. The format of this field is defined in .
2143:2112	U.3 = 514h M.2 = 258h E1.S = 258h	**Power State 2 Descriptor (PSD2):** This field indicates the characteristics of power state 2. The format of this field is defined in .
2175:2144	U.3 = 2BCh M.2 = 1F4h E1.S = 1F4h	**Power State 3 Descriptor (PSD3):** This field indicates the characteristics of power state 3. The format of this field is defined in .
2207:2176	190h	**Power State 4 Descriptor (PSD4):** This field indicates the characteristics of power state 4. The format of this field is defined in .

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Table 14: Identify – Identify Controller Data Structure

Bytes	Default Value	Description
4095:2208	–	Reserved.

Table 15: Power State Descriptor Data Structure

Bits	Description
15:0	**Maximum Power (MP):** This field indicates the maximum power consumed by the NVM subsystem in this power state. The power in Watts is equal to the value in this field multiplied by the scale specified in the Maximum Power Scale field.
23:16	Reserved.
24	**Max Power Scale (MXPS):** This field indicates the scale for the Maximum Power field in 0.01 Watts.
25	**Non-Operational State (NOPS):** This field indicates whether the controller processes I/O commands in this power state. If this field is cleared to 0, then the controller processes I/O commands in this power state. If this field is set to 1, then the controller does not process I/O commands in this power state.
31:26	Reserved.
63:32	**Entry Latency (ENLAT):** This field indicates the maximum entry latency in microseconds associated with entering this power state.
95:64	**Exit Latency (EXLAT):** This field indicates the maximum exit latency in microseconds associated with exiting this power state.
100:96	**Relative Read Throughput (RRT):** This field indicates the relative read throughput associated with this power state. A lower value means higher read throughput.
103:101	Reserved.
108:104	**Relative Read Latency (RRL):** This field indicates the relative READ latency associated with this power state. A lower value means lower READ latency.
111:109	Reserved.
116:112	**Relative Write Throughput (RWT):** This field indicates the relative write throughput associated with this power state. A lower value means higher write throughput.
119:117	Reserved.
124:120	**Relative Write Latency (RWL):** This field indicates the relative WRITE latency associated with this power state. A lower value means lower WRITE latency.
127:125	Reserved.
143:128	**Idle Power (IDLP):** This field indicates the typical power consumed by the NVM subsystem over 30 seconds in this power state when idle. The measurement starts after the NVM subsystem has been idle for 10 seconds. The power in Watts is equal to the value in this field multiplied by the scale indicated in the Idle Power Scale field.
149:144	Reserved.
151:150	**Idle Power Scale (IPS):** This field indicates the scale for the Idle Power field.
159:152	Reserved.
175:160	**Active Power (ACTP):** This field indicates the largest average power consumed by the NVM subsystem over a 10 second period in this power state with the workload indicated in the Active Power Workload field. The power in Watts is equal to the value in this field multiplied by the scale indicated in the Active Power Scale field.
178:176	**Active Power Workload (APW):** This field indicates the workload used to calculate maximum power for this power state.
181:179	Reserved.

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Table 15: Power State Descriptor Data Structure (Continued)

Bits	Description
183:182	**Active Power Scale (APS):** This field indicates the scale for the Active Power field.
255:184	Reserved.

Table 16: Identify – Identify Namespace Data Structure

Bits	Default Value	Description
07:00	Variable	**Namespace Size (NSZE):** This field indicates the total size of the namespace in logical blocks. A namespace of size *n* consists of LBA 0 through (*n* - 1). The number of logical blocks is based on the formatted LBA size.
15:08	Variable	**Namespace Capacity (NCAP):** This field indicates the maximum number of logical blocks that may be allocated in the namespace at any point in time. The number of logical blocks is based on the formatted LBA size. A logical block is allocated when it is written with a WRITE or WRITE UNCORRECTABLE command. A logical block may be deallocated using the DATASET MANAGEMENT command.
23:16	Variable	**Namespace Utilization (NUSE):** This field indicates the current number of logical blocks allocated in the namespace. This field is equal to the Namespace Capacity. The number of logical blocks is based on the formatted LBA size. When using the NVM command set: A logical block is allocated when it is written with a WRITE or WRITE UNCORRECTABLE command. A logical block may be deallocated using the DATASET MANAGEMENT command.
24	00010100b	**Namespace Features (NSFEAT):** This field defines features of the namespace. Bits 7:5: Reserved. Bit 4 = 1: The NPWG,NPWA, NPDG, NPDA, and NOWS are defined for this namespace and should be used by the host for IO optimization; And NOWS defined for this namespace shall adhere to Optimal Write Size field setting defined in NVM Sets Attributes Entry for the NVM Set with which this namespace is associated. Bit 3 = 0: The NGUID and EUI64 values can be reused by the controller to create a new namespace after the current namespace is deleted. Bit 2 = 1: The controller supports the deallocated or unwritten logical block error. Bit 1 = 0: The controller does not support the fields NAWUN, NAWUPF, and NACWU for the namespace. Bit 0 = 0: Thin provisioning is not supported, the Namespace Size and Namespace Capacity fields report the same value.
25	1	**Number of LBA Formats (NLBAF):** This field defines the number of supported LBA data sizes supported by the namespace. This is a 0s-based value.
26	Variable	**Formatted LBA Size (FLBAS):** This field indicates the LBA data size that the namespace has been formatted with. Bits 7:5: Reserved. Bit 4 = 0: The controller does not support metadata. Bits 3:0 = 0: Indicates a single supported LBA format.
27	0	**Metadata Capabilities (MC):** This field indicates the capabilities for metadata. Bits 7:2: Reserved. Bit 1 = 0: The namespace does not support the metadata being transferred as part of a separate buffer. Bit 0 = 0: The namespace does not support the metadata being transferred as part of an extended data LBA.

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Table 16: Identify – Identify Namespace Data Structure

Bits	Default Value	Description
28	0	**End-to-end Data Protection Capabilities (DPC):** This field indicates the capabilities for the end-to-end data protection feature. Bits 7:5: Reserved. Bit 4 = 0: The namespace does not support protection information transferred as the last eight bytes of metadata. Bit 3 = 0: The namespace does not support protection information transferred as the first eight bytes of metadata. Bit 2 = 0: The namespace does not support Protection Information Type 3. Bit 1 = 0: The namespace does not support Protection Information Type 2. Bit 0 = 0: The namespace does not support Protection Information Type 1.
29	Variable	**End-to-end Data Protection Type Settings (DPS):** This field indicates the Type settings for the end-to-end data protection feature. Bits 7:4: Reserved. Bit 3 = 0: Protection information, if enabled, is transferred as the last eight bytes of metadata. Bits 2:0 = 000b: Indicate whether Protection Information is enabled and the type of Protection Information enabled. The values for this field have the following meanings: 000b = Protection information is not enabled. 001b = Protection information is enabled, Type 1. 010b = Protection information is enabled, Type 2. 011b = Protection information is enabled, Type 3. 100b–111b = Reserved.
30	0	**Namespace Multi-path I/O and Namespace Sharing Capabilities (NMIC):** This field specifies multi-path I/O and namespace sharing capabilities of the namespace. Bits 7:1: Reserved. Bit 0 = 1: The namespace is a private namespace and is able to be attached to only one controller at a time.
31	0	**Reservation Capabilities (RESCAP):** Indicates the reservation capabilities of the namespace. Bit 7 = 0: Indicates that Ignore Existing Key is used as defined in revision 1.2.1 or earlier of this specification. Bit 6 = 0: Namespace does not support the Exclusive Access – All Registrants reservation type. Bit 5 = 0: Namespace does not support the Write Exclusive – All Registrants reservation type. Bit 4 = 0: Namespace does not support the Exclusive Access – Registrants Only reservation type. Bit 3 = 0: Namespace does not support the Write Exclusive –+ Registrants Only reservation type. Bit 2 = 0: Namespace does not support the Exclusive Access reservation type. Bit 1 = 0: Namespace does not support the Write Exclusive reservation type. Bit 0 = 0: Namespace does not support the Persist Through Power Loss capability.
32	Variable	**Format Progress Indicator (FPI):** If a format operation is in progress, this field indicates the percentage of the namespace that remains to be formatted. Bit 7 = 1: Indicates that the namespace supports the Format Progress Indicator defined by bits 6:0 in this field. Bits 6:0: Indicate the percentage of the Format NVM command that remains to be completed. If bit 7 is set to 1, then a value of 0h indicates that the namespace is formatted with the format specified by the FLBAS and DPS fields in this data structure and there is no Format NVM command in progress.

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Table 16: Identify – Identify Namespace Data Structure

Bits	Default Value	Description
33	00001001b	**Deallocate Logical Block Features (DLFEAT):** Indicates information about features that affect deallocating logical blocks for this namespace. Bits 7:5: Reserved. Bit 4 = 0: The guard field for the deallocated logical blocks that contain protection information is set to FFFFh. Bit 3 = 1: The controller does not support the deallocate bit in the WRITE ZEROS command for the namespace. Bits 2:0 = 1: Indicates the values read from a deallocated logical block and its metadata (excluding protection information).
35:34	0	**Namespace Atomic Write Unit Normal (NAWUN):** Namespace Atomic Write Unit Normal is not supported.
37:36	0	**Namespace Atomic Write Unit Power Fail (NAWUPF):** Namespace Atomic Write Unit Power Fail is not supported.
39:38	0	**Namespace Atomic Compare & Write Unit (NACWU):** Namespace Atomic Compare & Write Unit is not supported.
41:40	0	**Namespace Atomic Boundary Size Normal (NABSN):** Namespace Atomic Boundary Size Normal is not supported.
43:42	0	**Namespace Atomic Boundary Offset (NABO):** Namespace Atomic Boundary Offset is not supported.
45:44	0	**Namespace Atomic Boundary Size Power Fail (NABSPF):** Namespace Atomic Boundary Size Power Fail is not supported.
47:46	0	**Namespace Optimal IO Boundary (NOIOB):** Namespace Optimal IO Boundary is not reported.
63:48	Variable	**NVM Capacity (NVMCAP):** This field indicates the total size of the NVM allocated to this namespace. The value is in bytes.
65:64	128 or 32	**Namespace Preferred Write Granularity (NPWG):** This field indicates the smallest recommended write granularity in logical for this namespace. This is a 0's based value. The size indicated should be less than or equal to Maximum Data Transfer Size (MDTS) that is specified in units of minimum memory page size. The value of this field may change if the namespace is reformatted. The size should be a multiple of Namespace Preferred Write Alignment. (NPWA)
67:66	128 or 32	**Namespace Preferred Write Alignment (NPWA):** This field indicates the recommended write alignment in logical blocks for this namespace. This is a 0's based value. The value of this field may change if the namespace is reformatted.
69:68	128 or 32	**Namespace Preferred Deallocate Granularity (NPDG):** This field indicates the recommended granularity in logical blocks for the DATASET MANAGEMENT command with the Attribute - Deallocate bit set to 1 in Dword 11. This is a 0's based value. The value of this field may change if the namespace is reformatted. The size should be a multiple of Namespace Preferred Deallocate Alignment (NPDA).
71:70	128 or 32	**Namespace Preferred Deallocate Alignment (NPDA):** This field indicates the recommended alignment in logical blocks for the DATASET MANAGEMENT command with the Attribute - Deallocate bit set to 1 in Dword 11. This is a 0's based value. The value of this field may change if the namespace is reformatted.

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Table 16: Identify – Identify Namespace Data Structure

Bits	Default Value	Description
73:72	128 or 32	**Namespace Optimal Write Size (NOWS):** This field indicates the size in logical blocks for optimal write performance for this namespace. This is a 0's based value. The size indicated should be less than or equal to maximum data transfer size (MDTS) that is specified in units of minimum memory page size. The value of this may change if the namespace is reformatted. The value of this field should be a multiple of Namespace Preferred Write Granularity.
91:74	–	Reserved
95:92	0	**ANA Group Identifier (ANAGRPID):** This field indicates the ANA Group Identifier of the ANA Group of which the namespace is a member. Each namespace that is attached to a controller that supports Asymmetric Namespace Access Reporting shall report a valid ANAGRPID. If the controller does not support Asymmetric Namespace Access Reporting, then this field shall be cleared to 0h. If the value in this field changes and Asymmetric Namespace Access Change Notices are supported and enabled, then the controller shall issue an Asymmetric Namespace Access Change Notice.
98:96	–	Reserved
99	0	**Namespace Attributes (NSATTR):** This field specifies attributes of the namespace. Bits 7:1: Reserved. Bit 0: If se to 1, then the namespace is currently write protected due to any condition and all write access to the namespace shall fail. If cleared to 0, then the namespace is not currently write protected.
101:100	0	**NVM Set Identifier (NVMSETID):** This field indicates the NVM Set with which this namespace is associated. If NVM Sets are not supported by the controller, then this field shall be cleared to 0h.
103:102	0	**Endurance Group Identifier (ENDGID):** This field indicates the Endurance Group with which this namespace is associated. If Endurance Groups are not supported by the controller, then this field shall be cleared to 0h.
119:104	Variable	**Namespace Globally Unique Identifier (NGUID):** This field contains the 128-bit Namespace Globally Unique Identifier value.
127:120	Variable	**IEEE Extended Unique Identifier (EUI64):** This field contains the 64-bit IEEE Extended Unique Identifier value.
131:128	02090000h	**LBA Format 0 Support (LBAF0):** This field indicates the LBA format 0 that is supported by the controller. Bits 31:26: Reserved. Bits 25:24 = 0: Relative performance of the LBA format is not supported. Bits 23:16 = 09: Indicates the LBA data size supported; the value is reported in terms of a power of two (2^n) = 512-byte LBA data size. Bits 15:0 = 0: Metadata size is zero.
135:132	000C0000h	**LBA Format 1 Support (LBAF1):** This field indicates the LBA format 1 that is supported by the controller. Bits 31:26: Reserved. Bits 25:24 = 0: Relative performance of the LBA format is not supported. Bits 23:16 = 0C: Indicates the LBA data size supported; the value is reported in terms of a power of two (2^n) = 4096-byte LBA data size. Bits 15:0 = 0: Metadata size is zero.

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Table 16: Identify – Identify Namespace Data Structure

Bits	Default Value	Description
139:136	0	**LBA Format 2 Support (LBAF2):** This field indicates the LBA format 2 that is supported by the controller. Bits 31:26: Reserved. Bits 25:24 = 0: Relative performance of the LBA format is not supported. Bits 23:16 = 09: Indicates the LBA data size supported; the value is reported in terms of a power of two (2^n) = 512-byte LBA data size. Bits 15:0 = 8: Metadata size is eight.
143:140	0	**LBA Format 3 Support (LBAF3):** This field indicates the LBA format 3 that is supported by the controller. Bits 31:26: Reserved. Bits 25:24 = 0: Relative performance of the LBA format is not supported. Bits 23:16 = 0C: Indicates the LBA data size supported; the value is reported in terms of a power of two (2^n) = 4096-byte LBA data size. Bits 15:0 = 8: Metadata size is eight.
147:144	0	**LBA Format 4 Support (LBAF4):**This field indicates the LBA format 4 that is supported by the controller. Bits 31:26: Reserved. Bits 25:24 = 0: Relative performance of the LBA format is not supported. Bits 23:16 = 0C: Indicates the LBA data size supported; the value is reported in terms of a power of two (2^n) = 4096-byte LBA data size. Bits 15:0 = 40: Metadata size is sixty-four.
4095:148	–	Reserved.

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Commands

Table 17: Op Codes for Admin Commands

Codes not listed are reserved. All commands in the table are supported.

Command Name	Op Code (Hex)
DELETE I/O SUBMISSION QUEUE	00h
CREATE I/O SUBMISSION QUEUE	01h
GET LOG PAGE	02h
DELETE I/O COMPLETION QUEUE	04h
CREATE I/O COMPLETION QUEUE	05h
IDENTIFY	06h
ABORT	08h
SET FEATURES - SET ARBITRATION	09h - 01h
SET FEATURES - SET POWER MANAGEMENT	09h - 02h
SET FEATURES - SET TEMPERATURE THRESHOLD	09h - 04h
SET FEATURES - SET ERROR RECOVERY	09h - 05h
SET FEATURES - SET NUMBER OF QUEUES	09h - 07h
SET FEATURES - SET INTERRUPT COALESCE	09h - 08h
SET FEATURES - SET INTERRUPT VECTOR CONFIGURATION	09h - 09h
SET FEATURES - SET WRITE ATOMICITY	09h - 0Ah
SET FEATURES - SET ASYNC EVENT CONFIGURATION	09h - 0Bh
SET FEATURES - HOST CONTROLLED THERMAL MANAGEMENT	09h - 10h
SET FEATURES - SANITIZE CONFIGURATION	09h - 17h
SET FEATURES - SW PROGRESS MARKER	09h - 80h
SET FEATURES - DEVICE INITIATED THERMAL THROTTLING	09h - D4h
GET FEATURES - GET ARBITRATION	0Ah - 01h
GET FEATURES - GET POWER MANAGEMENT	0Ah - 02h
GET FEATURES - GET TEMPERATURE THRESHOLD	0Ah - 04h
GET FEATURES - GET ERROR RECOVERY	0Ah - 05h
GET FEATURES - GET NUMBER OF QUEUES	0Ah - 07h
GET FEATURES - GET INTERRUPT COALESCE	0Ah - 08h
GET FEATURES - GET INTERRUPT VECTOR CONFIGURATION	0Ah - 09h
GET FEATURES - GET WRITE ATOMICITY	0Ah - 0Ah
GET FEATURES - GET ASYNC EVENT CONFIGURATION	0Ah - 0Bh
GET FEATURES - HOST CONTROLLED THERMAL MANAGEMENT	0Ah - 10h
GET FEATURES - SANITIZE CONFIGURATION	0Ah - 17h
GET FEATURES - SW PROGRESS MARKER	0Ah - 80h
GET FEATURES - DEVICE INITIATED THERMAL THROTTLING	0Ah - D4h
ASYNCHRONOUS EVENT REQUEST	0Ch

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Command Name	Op Code (Hex)
NAMESPACE MANAGEMENT	0Dh
FIRMWARE COMMIT	10h
FIRMWARE IMAGE DOWNLOAD	11h
DEVICE SELF TEST (DST)	14h
NVME - MI SEND	1Dh
NVME - MI RECEIVE	1Eh
NAMESPACE ATTACHMENT	15h
FORMAT NVM	80h
SECURITY SEND	81h
SECURITY RECEIVE	82h
SANITIZE	84h

Table 18: Op Codes for NVMe Commands

Codes not listed are reserved. All commands in the table are supported.

Command Name	Op Code (Hex)
FLUSH	00h
WRITE	01h
READ	02h
DATASET MANAGEMENT – DEALLOCATE (AD)	09h
WRITE UNCORRECTABLE	04h
COMPARE	05h
WRITE ZEROS	08h

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Log Pages

The Micron 7400 SSD supports log information as defined in the NVMe specification. Supported information is shown in the following tables:

- Error Information (Log Identifier 01h)
- SMART/Health Information (Log Identifier 02h)
- Firmware Slot Information (Log Identifier 03h)
- Changed Namespace List (Log Identifier 04h)
- Commands Supported and Effects (Log Identifier 05h)
- Device Self-Test (Log Identifier 06h)
- Telemetry Host-Initiated (Log Identifier 07h)
- Telemetry Controller-Initiated (Log Identifier 08h)
- Persistent Event Log (Log Identifier 0Dh)
- Reservation Notification (Log Identifier 80h)
- Sanitize Status (Log Identifier 81h)
- Micron Vendor Unique SMART (Log Identifier CAh)
- Micron SMART Extended Health Information Log (Log Identifier D0h)

Table 19: Error Information (Log Identifier 01h)

Bytes	Name	Description
7:0	Error count	This is a 64-bit incrementing error count, indicating a unique identifier for this error. The error count starts at 1h, is incremented for each unique error log entry, and is retained across power off conditions. A value of 0h indicates an invalid entry; This value may be used when there are lost entries or when there are fewer errors than the maximum number of entries the controller supports.
9:8	Submission queue ID	This field indicates the submission queue Identifier of the command that the error information is associated with. If the error is not specific to a particular command then this field shall be set to FFFFh.
11:10	Command ID	This field indicates the command Identifier of the command that the error is associated with. If the error is not specific to a particular command then this field shall be set to FFFFh.
13:12	Status field	This field indicates the status field for the command that completed. The status field is located in bits 15:01, bit 00 corresponds to the phase tag posted for the command. If the error is not specific to a particular command then this field reports the most applicable status value.
15:14	Parameter error location	This field indicates the byte and bit of the command parameter that the error is associated with, if applicable. If the parameter spans multiple bytes or bits, then the location indicates the first byte and bit of the parameter. Bit 7:0: Byte in command that contained the error. Valid values are 0 to 63. Bit 10:8: Bit in command that contained the error. Valid values are 0 to 7. Bit 15:11: Reserved If the error is not specific to a particular command then this field shall be set to FFFFh.
23:16	LBA	This field indicates the first LBA that experienced the error condition, if applicable.
27:24	Namespace	This field indicates the namespace that the error is associated with, if applicable.
31:28	Reserved	Reserved.

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Table 19: Error Information (Log Identifier 01h) (Continued)

Bytes	Name	Description
39:32	Command specific information	This field contains command specific information. If used, the command definition specifies the information returned.
63:40	Reserved	Reserved.

Table 20: SMART/Health Information (Log Identifier 02h)

Bytes	Name	Description
0	Critical warning	Indicates critical warnings for the state of the controller. Each bit corresponds to a critical warning type; Multiple bits may be set. If a bit is cleared to 0, the critical warning does not apply. Critical warnings may result in an asynchronous event notification to the host. Bit 0: If set to 1, the available spare space has fallen below the threshold. Bit 1: If set to 1, the temperature has exceeded a critical threshold. Bit 2: If set to 1, the device reliability has been degraded due to significant media-related errors or any internal error that degrades device reliability. Bit 3: If set to 1, the media has been placed in read-only mode. Bits 7:4: Reserved
2:1	Composite temperature	Contains the temperature of the overall device (controller and NVM included) in units of Kelvin. If it exceeds the temperature threshold, an asynchronous event may be issued to the host.
3	Available spare	Contains a normalized percentage (0-100%) of the remaining available spare capacity.
4	Available spare threshold	When the available spare falls below the threshold indicated in this field, an asynchronous event may be issued to the host. The value is indicated as a normalized percentage (0-100%).
5	Percentage used	Contains an estimate of the percentage of the device life used based on the actual device usage and prediction of device life. A value of 100 indicates that the estimated endurance of the device has been consumed, but may not indicate a device failure. The value is allowed to exceed 100.
		Percentages greater than 254 shall be represented as 255. This value shall be updated once per power-on hour (when the controller is not in a sleep state).
31:6	Reserved	Reserved.
47:32	Data units read	Contains the number of 512 byte data units the host has read from the controller; This value does not include metadata. This value is reported in thousands (that is, a value of 1 corresponds to 1000 units of 512 bytes read) and is rounded up. For the NVM command set, logical blocks read as part of COMPARE and READ operations shall be included in this value.
63:48	Data units written	Contains the number of 512 byte data units the host has written to the controller; This value does not include metadata. This value is reported in thousands (that is, a value of 1 corresponds to 1000 units of 512 bytes written) and is rounded up. For the NVM command set, logical blocks written as part of WRITE operations shall be included in this value.
79:64	Host READ commands	Contains the number of READ commands completed by the controller. For the NVM command set, this is the number of COMPARE and READ commands.
95:80	Host WRITE commands	Contains the number of WRITE commands completed by the controller. For the NVM command set, this is the number of WRITE commands.

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Table 20: SMART/Health Information (Log Identifier 02h) (Continued)

Bytes	Name	Description
111:96	Controller busy time	Contains the amount of time the controller is busy with I/O commands. The controller is busy when there is a command outstanding to an I/O queue (specifically, a command was issued via an I/O submission queue tail doorbell write and the corresponding completion queue entry has not been posted yet to the associated I/O completion queue. This value is reported in minutes.
127:112	Power cycles	Contains the number of power cycles.
143:128	Power on hours	Contains the number of power-on hours. This does not include time that the controller was powered and in a low-power state condition.
159:144	Unsafe shutdowns	Contains the number of unsafe shutdowns. This count is incremented when a shutdown notification (CC.SHN) is not received prior to loss of power.
175:160	Media and data integrity errors	Contains the number of occurrences where the controller detected an unrecovered data integrity error.
191:176	Number of error info log entries	Contains the number of error information log entries over the life of the controller.
195:192	Warning composite temperature time	Contains the amount of time in minutes that the controller is operational and the composite temperature is greater than or equal to the warning composite temperature threshold (WCTEMP) field and less than the critical composite temperature threshold (CCTEMP) field in the Identify controller data structure.
199:196	Critical composite temperature time	Contains the amount of time in minutes that the controller is operational and the composite temperature is greater the critical composite temperature threshold (CCTEMP) field in the Identify controller data structure.
201:200	Temperature Sensor 1	Contains the current temperature reported by temperature sensor 1.
203:202	Temperature Sensor 2	Contains the current temperature reported by temperature sensor 2.
511:204	Reserved	Reserved

Table 21: Firmware Slot Information (Log Identifier 03h)

Bytes	Name	Description
0	Active Firmware Info (AFI)	Specifies information about the active firmware revision. Bit 7 is reserved Bits 6:4 indicates the firmware slot that is going to be activated at the next controller reset. Bit 3 is reserved Bits 2:0 indicates the firmware slot from which the actively running firmware revision was loaded.
7:1	Reserved	Reserved.
15:8	Firmware Revision for Slot 1 (FRS1)	Contains the revision of the firmware downloaded to firmware slot 1. Firmware slot is read-only.
23:16	Firmware Revision for Slot 2 (FRS2)	Contains the revision of the firmware downloaded to firmware slot 2.
31:24	Firmware Revision for Slot 3 (FRS3)	Contains the revision of the firmware downloaded to firmware slot 3.
511:32	Reserved	Reserved.

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Log Identifier 04h

Changed Namespace List (Log Identifier 04h)

This log page is used to describe namespaces attached to this controller that have:

- Changed information in their Identify Namespace data structure since the last time the log pagewas read;
- been added; and
- been deleted.

The log page contains a Namespace List with up to 1,024 entries. If more than 1,024 namespaces have changed attributes since the last time the log was read, the first entry in the log page shall be set to FFFFFFFFh and the remainder of the list shall be zero filled.

Table 22: Commands Supported and Effects (Log Identifier 05h)

Bytes	Name	Description
3:0	Admin Command Supported 0 (ACS0)	Contains the Command Effect data structure for the Admin command with an opcode value of 0h. The format of this field is defined by the NVM Express specification.
⋮	⋮	⋮
1023:1020	Admin Command Supported 255 (ACS255)	Contains the Command Effect data structure for the Admin command with an opcode value of 255. The format of this field is defined by the NVM Express specification.
1027:1024	I/O Command Supported 0 (IOCS0)	Contains the Command Effect data structure for the I/O command with an opcode value of 0h. The format of this field is defined by the NVM Express specification.
⋮	⋮	⋮
2047:2044	I/O Command Supported 255 (IOCS255)	Contains the Command Effect data structure for the I/O command with an opcode value of 255. The format of this field is defined by the NVM Express specification.
4095:2048	Reserved	Reserved.

Table 23: Get Log Page – Device Self-Test Log (Log Identifier 06h)

Bytes	Name	Description
0	Current Device Self-Test Operation	Bits 7-4: Reserved. Bits 3-0: Indicates the status of the current device self-test operation as defined below: 3h~Fh: Reserved. 2h: Extended device self-test operation in progress. 1h: Short device self-test operation in progress. 0h: No device self-test operation in progress.
1	Current Device Self-Test Completion	Bit 7: Reserved. Bits 6-0: Indicates the percentage of the device self-test operation. Note: If bits 3-0 in the Current Device Self-Test Operation field are set to 0h, then this field is ignored.
3:2	Reserved	–

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Table 23: Get Log Page – Device Self-Test Log (Log Identifier 06h)

Bytes	Name	Description
31:4	Newest Self-Test Result	Byte 25: Status code. Byte: 24: Status code type. Bytes 23-16: Failing LBA. Bytes 15-12: Namespace identifier (NSID). Bytes 11-4: Power-on hours. Byte 3: Reserved. Byte 2: Valid diagnostic information. Byte 1: Segment number. Byte 0: Device self-test status.
59:32	2nd-Newest Self-Test Result	Same as above.
.....	.....	Same as above.
535:508	19th-Newest Self-Test Result	Same as above.
563:536	20th-Newest Self-Test Result	Same as above.

Table 24: Telemetry Host-Initiated (Log Identifier 07h)

Bytes	Name	Description
0	Log Identifier	This field shall be set to 07h.
4:1	RSVP	Reserved.
7:5	IEEE OUI Identifier (IEEE)	Contains the Organization Unique Identifier (OUI) for the controller vendor that is able to interpret the data. If cleared to 0h, no IEEE OUI Identifier is present.
9:8	Telemetry Host-Initiated Data Area 1 Last Block	Contains the value of the last block of Telemetry Host- Initiated Data Area 1. If the Telemetry Host-Initiated Data Area 1 does not contain data, then this field shall be cleared to 0h. If this field is not 0h, then Telemetry Host-Initiated Data Area 1 begins at block 1h and ends at the block contained in this field.
11:10	Telemetry Host-Initiated Data Area 2 Last Block	Contains the value of the last block of Telemetry Host- Initiated Data Area 2. This value shall be greater than or equal to the value in the value in the Telemetry Host-Initiated Data Area 1 Last Block field. If this field is not 0h, then Telemetry Host-Initiated Data Area 2 begins at block 1h and ends at the block contained in this field.
13:12	Telemetry Host-Initiated Data Area 3 Last Block	Contains the value of the last block of Telemetry Host- Initiated Data Area 3. This value shall be greater than or equal to the value in the value in the Telemetry Host-Initiated Data Area 2 Last Block field. If this field is not 0h, then Telemetry Host-Initiated Data Area 3 begins at block 1h and ends at the block contained in this field.
381:14	RSVP	Reserved
382	Telemetry Controller-Initiated Data Available	Contains the value of the Telemetry Controller-Initiated Data Available field in the Telemetry Controller-Initiated log.
383	Telemetry Controller-Initiated Data Generation Number	Contains the value of the Telemetry Controller-Initiated Data Generation Number field in the Telemetry Controller-Initiated log.
511:384	Reason Identifier	Contains a vendor-specific identifier that describes the operating conditions of the controller at the time of capture. The Reason Identifier field should provide an identification of unique operating conditions of the controller.

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Table 24: Telemetry Host-Initiated (Log Identifier 07h) (Continued)

Bytes	Name	Description
1023:512	Telemetry Host-Initiated Data Block 1	Contains Telemetry Data Block 1 for the Telemetry Host-Initiated Log.
1535:1024	Telemetry Host-Initiated Data Block 2	Contains Telemetry Data Block 2 for the Telemetry Host-Initiated Log.
⋮	⋮	⋮
(n*512) + 511: (n*512)	Telemetry Host-Initiated Data Block n	Contains Telemetry Data Block n for the Telemetry Host-Initiated Log.

Table 25: Telemetry Controller-Initiated (Log Identifier 08h)

Bytes	Name	Description
0	Log Identifier	This field shall be set to 08h.
4:1	RSVP	Reserved.
7:5	IEEE OUI Identifier (IEEE)	Contains the Organization Unique Identifier (OUI) for the controller vendor that is able to interpret the data. If cleared to 0h, no IEEE OUI Identifier is present.
9:8	Telemetry Controller-Initiated Data Area 1 Last Block	Contains the value of the last block of Telemetry Host- Initiated Data Area 1. If the Telemetry Controller-Initiated Data Area 1 does not contain data, then this field shall be cleared to 0h. If this field is not 0h, then Telemetry Controller-Initiated Data Area 1 begins at block 1h and ends at the block contained in this field.
11:10	Telemetry Controller-Initiated Data Area 2 Last Block	Contains the value of the last block of Telemetry Controller- Initiated Data Area 2. This value shall be greater than or equal to the value in the value in the Telemetry Controller- Initiated Data Area 1 Last Block field. If this field is not 0h, then Telemetry Controller-Initiated Data Area 2 begins at block 1h and ends at the block contained in this field.
13:12	Telemetry Controller-Initiated Data Area 3 Last Block	Contains the value of the last block of Telemetry Controller- Initiated Data Area 3. This value shall be greater than or equal to the value in the value in the Telemetry Controller- Initiated Data Area 2 Last Block field. If this field is not 0h, then Telemetry Controller-Initiated Data Area 3 begins at block 1h and ends at the block contained in this field.
381:14	RSVP	Reserved.
382	Telemetry Controller-Initiated Data Available	If this field is cleared to 0h, the log does not contain saved internal controller state. If this field is set to 1h, the log contains saved internal controller state. If this field is set to 1h, it shall not be cleared to 0h until a Get Log Page command with Retain Asynchronous Event bit cleared to '0' for the Telemetry Controller-Initiated log completes successfully. This value is persistent across power states and reset.
383	Telemetry Controller-Initiated Data Generation Number	Contains a value that is incremented each time the controller initiates a capture of its internal controller state into the Telemetry Controller-Initiated Data Blocks. If the value of this field is FFh, then the field shall be cleared to 0h when incremented. This field is persistent across power on.
511:384	Reason Identifier	Contains a vendor-specific identifier that describes the operating conditions of the controller at the time of capture. The Reason Identifier field should provide an identification of unique operating conditions of the controller.
1023:512	Telemetry Host-Initiated Data Block 1	Contains Telemetry Data Block 1 for the Telemetry Controller-Initiated Log captured at a vendor-specific time.
1535:1024	Telemetry Host-Initiated Data Block 2	Contains Telemetry Data Block 2 for the Telemetry Controller-Initiated Log captured at a vendor-specific time.

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Table 25: Telemetry Controller-Initiated (Log Identifier 08h) (Continued)

Bytes	Name	Description
⋮	⋮	⋮
(n*512) + 511: (n*512)	Telemetry Host-Initiated Data Block n	Contains Telemetry Data Block n for the Telemetry Controller-Initiated Log captured at a vendor-specific time.

Table 26: Persistent Event Log (Log Identifier 0Dh)

Bytes	Name	Description
0	Log Identifier	This field shall be set to 0Dh.
3:1	RSVD	Reserved.
7:4	Total Number of Events	Contains the number of the event entries in the log.
15:8	Total Log Length	Contains the total number of bytes of persistent event log page data available, including the header.
16	Log Revision	Contains a number indicating the revision of the Get Log Page data structure that this log page a data complies with. Shall be set to 01h.
17	RSVD	Reserved.
19:18	Log Header Length	This field contains the length in bytes of te log header information that follows. The total length of the log header in bytes is the value in this field plus 20.
27:20	Timestamp	Shall return a timestamp using the format Timestamp.
43:28	Power on Hours (POH)	This field indicates the number of power-on hours at the time the Persistent Event log was retrieved. This may not include time that the controller was powered and in a non-operational state.
51:44	Power Cycle Count	Contains the number of power cycles for this controller.
53:52	PCI Vendor ID (VID)	This is the same value as reported in the Identify Controller data structure PCI Vendor ID field.
55:54	PCI Subsystem Vendor ID (SSVID)	This is the same value as reported in the Identify Controller data structure PCI Subsystem Vendor ID field.
75:56	Serial Number	This field contains the same value as reported in the Serial Number field of the Identify Controller data structure, bytes 23:04.
115:76	Model Number	This field contains the same value as reported in the Model Number field of the Identify Controller data structure, bytes 63:24.
371:116	NVM Subsystem NVMe Qualified Name (SUBNQN)	This field contains the same value as reported in the NVM Subsystem NVMe Qualified Name field of the Identify Controller data structure, bytes 1023:768. If the NVM Subsystem NVMe Qualified Name field of the Identify Controller data structure is not supported, then all bytes of this field shall be cleared to 0h.
479:372	RSVD	Reserved.
511:480	Supported Events Bitmap	This field contains a bitmap indicating support for the persistent event log events. Each bit in the bitmap corresponds to the value for the event type. A bit set to 1 indicates that the corresponding event is supported. A bit cleared to 0 indicates that the corresponding event is not supported.
(M - 1) + 512 :512	Persistent Event 0	This field contains the first persistent event log entry where M is the length of this persistent event.
⋮	⋮	⋮

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Table 26: Persistent Event Log (Log Identifier 0Dh) (Continued)

Bytes	Name	Description
(TLL - 1) :(TLL - K)	Persistent Event N	This field contains the last persistent event log entry where K is the length of this persistent event and TLL is the size specified in the Total Log Length field.

Table 27: Reservation Notification (Log Identifier 80h)

Bytes	Name	Description
7:0	Log Page Count	This is a 64-bit incrementing reservation notification log page count, indicating a unique identifier for this notification. The count starts at 0h following a controller reset, is incremented with each unique log entry, and rolls over to zero when the maximum count is reached and a log page is created. A value of 0h indicates an empty log entry.
8	Reservation Notification Log Page Type	This field indicates the Reservation Notification type described by this log page. 0 = Empty log page. GET LOG PAGE command was processed when no unread reservation notification log pages were available. All the fields of an empty log page shall have a value of zero. 1 = Registration preempted. 2 = Reservation released. 3 = Reservation preempted. 255:4 = Reserved.
9	Number of Available Log Pages	This field indicates the number of additional available reservation notification log pages (that is, the number of unread log pages, not counting this one). If there are more than 255 additional available log pages, then a value of 255 is returned. A value of zero indicates that there are no additional available log pages.
11:10	Reserved	Reserved.
15:12	Namespace ID	This field indicates the namespace ID of the namespace associated with the reservation notification described by this log page.
63:16	Reserved	Reserved.

Table 28: Sanitize Status (Log Identifier 81h)

Bytes	Name	Description
1:0	Sanitize Progress (SPROG)	This field indicates the fraction complete of the sanitize operation. The value is a numerator of the fraction complete that has 65,536 (10000h) as its denominator. This value shall be set to FFFFh if bits 2:0 of the SSTAT field are not set to 010b. If a SANITIZE operation has been started by a SANITIZE command with the No-Deallocate After Sanitize bit set to 1 and if NODMMAS field in the Identify Controller data structure is set to 10b, then the fraction reported shall include the time related to the additional media modification.
3:2	Sanitize Status (SSTAT)	This field indicates the status associated with the most recent sanitize operation. Bits 15:9: Reserved. Bit 8 (Global Data Erased): If set to 1, then no namespace logical block in the NVM subsystem has been written to and no Persistent Memory Region in the NVM subsystem has been enabled. If cleared to 0, then a namespace logical block in the NVM subsystem has been written to or a Persistent Memory Region in the NVM subsystem has been enabled. Bits 7:3: Contains the number of completed passes if the most recent sanitize operation was an Overwrite. This field shall be cleared to 0h if the most recent sanitize operation was not an OVerwrite. Bits 2:0: Contains the status of the most recent SANITIZE operation as SANITIZE Operation Table.

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Table 28: Sanitize Status (Log Identifier 81h) (Continued)

Bytes	Name	Description
7:4	Sanitize Command Dword 10 Information	This field contains the value of the Command Dword 10 field of the SANITIZE command that started the SANITIZE operation whose status is reported in the SSTAT field.
11:8	Estimated Time For Overwrite	This field indicates the number of seconds required to complete an Overwrite SANITIZE operation with 16 passes in the background when the No-Deallocate Modifies Media After Sanitize field is not set to 10b. A value of 0h indicates that the SANITIZE operation is expected to be completed in the background when the SANITIZE command that started that operation is completed. A value of FFFFFFFFh indicates that no time period is reported.
15:12	Estimated Time For Block Erase	This field indicates the number of seconds required to complete a Block Erase SANITIZE operation in the background when the No-Deallocate Modifies Media After Sanitize field is not set to 10b. A value of 0h indicates that the SANITIZE operation is expected to be completed in the background when the SANITIZE command that started that operation is completed. A value of FFFFFFFFh indicates that no time period is reported.
19:16	Estimated Time For Crypto Erase	This field indicates the number of seconds required to complete a Crypto Erase SANITIZE operation in the background when the No-Deallocate Modifies Media After Sanitize field is not set to 10b. A value of 0h indicates that the SANITIZE operation is expected to be completed in the background when the SANITIZE command that started that operation is completed. A value of FFFFFFFFh indicates that no time period is reported.
23:20	Estimated Time For Overwrite With No-Deallocate Media Modification	This field indicates the number of seconds required to complete an Overwrite SANITIZE operation and the associated additional media modification after the Overwrite SANITIZE operation in the background when: a) the No-Deallocate bit was set to 1 in the SANITIZE command that requested the Overwrite SANITIZE operation; and b) the No-Deallocate Modifies Media After Sanitize field is set to 10b. A value of 0h indicates that the SANITIZE operation is expected to be completed in the background when the SANITIZE command that started that operation is completed. A value of FFFFFFFFh indicates that no time period is reported.
27:24	Estimated Time For Block Erase With No-Deallocate Media Modification	This field indicates the number of seconds required to complete a Block Erase SANITIZE operation and the associated additional media modification after the Block Erase SANITIZE operation in the background when: a) the No-Deallocate bit was set to 1 in the SANITIZE command that requested the Block Erase SANITIZE operation; and b) the No-Deallocate Modifies Media After Sanitize field is set to 10b. A value of 0h indicates that the SANITIZE operation is expected to be completed in the background when the SANITIZE command that started that operation is completed. A value of FFFFFFFFh indicates that no time period is reported.
31:28	Estimated Time For Crypto Erase With No-Deallocate Media Modification	This field indicates the number of seconds required to complete a Crypto Erase SANITIZE operation and the associated additional media modification after the Crypto Erase SANITIZE operation in the background when: a) the No-Deallocate bit was set to 1 in the SANITIZE command that requested the Crypto Erase SANITIZE operation; and b) the No-Deallocate Modifies Media After Sanitize field is set to 10b. A value of 0h indicates that the SANITIZE operation is expected to be completed in the background when the SANITIZE command that started that operation is completed. A value of FFFFFFFFh indicates that no time period is reported.
511:32	RSVD	Reserved

Table 29: SANITIZE Operation Table

Value	Definition
000b	The NVM subsystem has never been sanitized.
001b	The most recent SANITIZE operation completed successfully including any additional media modification.

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Table 29: SANITIZE Operation Table (Continued)

Value	Definition
010b	A SANITIZE operation is currently in progress.
011b	The most recent SANITIZE operation failed.
100b	The most recent SANITIZE operation for which No-Deallocate After Sanitize was requested has completed successfully with deallocation of all LBAs.

Table 30: Micron Vendor Unique SMART (Log Identifier CAh)

Bytes	Name	Description
0	F9h	**Total NAND writes:** Reports the cumulative number of writes to NAND in 1GB increments.
4:1	Reserved	
11:5	Total NAND writes	
12	FAh	**Total NAND reads**: Reports the cumulative number of reads from NAND in 1GB increments.
16:13	Reserved	
23:17	Total NAND reads	
24	EAh	**Thermal throttle status and time:** Reports the current throttle status and total throttling time. Byte 29: If set to 1, throttling is active; If set to 0, throttling is not active Bytes 34:30 = Total throttling time in minutes since power on
28:25	Reserved	
34:29	Thermal throttle status and time	
35	Reserved	
36	E7h	**Lifetime temperature:** Reports the maximum and minimum temperature in degrees Kelvin over the lifetime of the drive. Bytes 42:41 = Maximum temperature Bytes 44:43 = Minimum temperature Bytes 46:45 = Current temperature
40:37	Reserved	
46:41	Lifetime temperature	
47	Reserved	
48	E8h	**Power consumption:** Reports the maximum, minimum, and average power consumption in watts. Bytes 54:53 = Maximum power consumption Bytes 56:55 = Minimum power consumption Bytes 58:57 = Average power consumption
52:49	Reserved	
58:53	Power consumption	
59	Reserved	
60	AFh	**Power on temperature:** Reports the maximum and minimum temperature in degrees Kelvin since the last power on. Bytes 66:65 = Maximum temperature Bytes 68:67 = Minimum temperature Bytes 70:69 = Current temperature
64:61	Reserved	
70:65	Power on temperature	
71	Reserved	

Table 31: Micron Extended SMART Log (Log Identifier D0h)

Bytes	Name	Description
11:0	Reserved	Reserved
15:12	Grown Bad Block Count	Total number of Retired Bad Blocks since the drive has left manufacturing. Retired Blocks are NAND blocks that are not used during normal firmware operation and may include both bad blocks and good blocks. An example of where a good block may be retired is when a Super Block is marked bad (for example, not enough good blocks for RAIN correction or not enough good blocks to have each target parallelism for performance).

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Table 31: Micron Extended SMART Log (Log Identifier D0h) (Continued)

Bytes	Name	Description
19:16	Per Block Max Erase Count	Highest erase count of any Flash block on any chip on the drive.
23:20	Power On (Minutes)	IMPLEMENT as Use Power-on hrs* 60. Update Frequency once per hour
47:24	Reserved	Reserved
51:48	Write Protect Reason	The reasons for entering Write Protect Mode. Bit 0: DRAM double bit error Bit 1: Low remaining spare block count Bit 2: Power holdup capacitor failure Bit 3: NVRAM checksum failure Bit 4: DRAM address out of range Bit 5: Overtemp shutdown Bits 31:6: Reserved
63:52	Reserved	Reserved
71:64	Device Capacity	Total full device capacity
79:72	Reserved	Reserved
87:80	Total Erase Count	Total erase count across all flash blocks on the drive
95:88	Lifetime Use Rate	Erase count over time which equals to Total Erase Count (87:80)/Power On Time (23:20)
207:96	Reserved	Reserved
211:208	Translation Unit Size	Represents the Translation Unit Size of the drive
215:212	Total Block Stripe Count for User Data - TLC/QLC	Represents the number of TLC/QLC Block Stripes allocated for user data on the drive.
219:216	Free Block Stripe Count for User Data - TLC/QLC	Represents the number of Free TLC/QLC Block Stripes allocated for user data on the drive.
227:220	Block Stripe Size - TLC/QLC (User Data)	Represents the approximate amount of User Data (in bytes) that can be stored in a TLC/QLC NAND Block Stripe.
243:228	Reserved	Reserved
247:244	User Block Min Erase Count	Lowest erase count of any user data Flash block on any chip on the drive.
251:248	User Block Average Erase Count	Average erase count across all user data Flash blocks on the drive
255:252	User Block Max Erase Count	Max erase count across all user data Flash blocks on the drive

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SMBus Out-of-Band Management

SMBus Sideband Management

The Micron 7400 SSD Series uses the SMBus interface for presenting product data, monitoring drive health, checking drive status before power-up, and error posting.

Protocol supported: Enterprise SSD form factor interface with its accompanying vital product data (VPD) definition.

Management data and vital product data can be accessed at fixed addresses with +3.3V_{AUX} (U.3/EDSFF form factor) prior to powering up the drive completely. This data continues to be available at this fixed address when the drive is fully powered up. MCTP utilizes the SMBus to perform transactions between the NVMe subsystem/endpoints with the MCTP package.

MCTP

The Micron 7400 SSD Series is fully compliant with NVMe-MI 1.1a. In addition to mandatory NVMe-MI and admin commands, the 7400 offers the following optional admin commands: SET FEATURE, NAMESPACE MANAGEMENT, and FIRMWARE ACTIVATE/COMMIT commands.

Table 32: Out-of-Band Management Details

Out-of-Band Specification	SMBus Address	Alternate Address (Due to Bit Shift)	Out-of-Band Data Structure
Enterprise SSD form factor	0x53	0xA6	Vital product data (VPD)
NVMe management interface	0x6A	0xD4	Subsystem management data (SMD)
	0x3A	0x1D	Management component transport protocol (MCTP)

Notes: 1. SMBus addresses will appear at an alternate address in certain tools due the inclusion of direction bit in the SMBus spec.
2. Out-of-band management is enabled by default.

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Table 33: Vital Product Data (VPD) Structure

Address	#Bytes	Function	Value	Byte Offset	Description
0x53 (7-bit)	3	Class code	02h	0	Device type and programming interface
			08h	1	
			01h	2	
	2	ID	44h	3	PCI-SIG vendor ID
			13h	4	
	20		Variable	5–24	Serial number
	40		Variable	25–64	Model number
	1	PCIe port0 capabilities	03h	65	Maximum link speed
	1		04h	66	Maximum link width
	1	PCIe port1 capabilities	03h	67	Maximum link speed
	1		02h	68	Maximum link width
	1	Initial power requirements	08h	69	12V power rail initial power requirement (W)
	2	Reserved	0	70–71	Reserved
	1	Maximum power require-ments	24h	72	12V power rail maximum power require-ment (W)
	2	Reserved	0	73–74	Reserved
	2	Capability list pointer	4Dh	75	16b address offset pointers to start of capability list; see Capability List Pointer table
			00h	76	

Table 34: Capability List Pointer

Address	#Bytes	Value	Byte Offset	R/W	Description
0x004D	2	A5h	0	RO	PCI-SIG vendor-specific capability
		00h	1		
	2	00h	2	RO	Pointer to next capability
		00h	3		
	2	44h	4	RO	PCI-SIG vendor ID (0x1344 is assigned to Micron)
		13h	5		
	2	0000h	6–7	RO	Reserved
	2	Variable	8	RO	Temperature value (Celsius), little-endian
		Variable	9		

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Table 35: Subsystem Management Data (SMD) Structure

Address	#Bytes	Value	Byte Offset	Description
0x6A (7-bit)	1	06h	0	**Length of Status:** Indicates number of additional bytes to read before encountering PEC.
	1	Variable	1	**Status Flags (SFLGS):** Indicates the status of the NVM subsystem.
				SMBus Arbitration: Bit 7 is set to 1 after an SMBus block read is completed all the way to the stop bit without bus contention and cleared to 0 if an SMBus send byte FFh is received on this SMBus slave address.
				Drive Not Ready: Bit 6 is set to 1 when the subsystem is not capable of processing NVMe management commands, and the rest of the transmission may be invalid. If cleared to 0, then the NVM subsystem is fully powered and ready to respond to management commands. This logic level intentionally identifies and prioritizes powered up and ready drives over their powered off neighbors on the same SMBus segment.
				Drive Functional: Bit 5 is set to 1 to indicate an NVM subsystem is functional. If cleared to 0, then there is an unrecoverable failure in the NVM subsystem and the rest of the transmission may be invalid.
				Reset Not Required: Bit 4 is set to 1 to indicate the NVM subsystem does not need a reset to resume normal operation. If cleared to 0 then the NVM subsystem has experienced an error that prevents continued normal operation. A controller level reset is required to resume normal operation.
				Port 0 PCIe Link Active: Bit 3 is set to 1 to indicate the first port's PCIe link is up (that is, the data link control and management state machine is in the DL_Active state). If cleared to 0, then the PCIe link is down.
				Port 1 PCIe Link Active: Bit 2 is cleared to 0, the second port's PCIe link is not present.
	1	Variable	2	**SMART Warnings:** This field shall contain the critical warning field (byte 0) of the NVMe SMART/Health Information log. Each bit in this field shall be inverted from the NVMe definition (that is, the management interface shall indicate a 0 value while the corresponding bit is 1 in the log page). Refer to the NVMe specification for bit definitions. Cleared to 0 if the NVM subsystem indicates a critical warning for the corresponding bit. Set to 1 if the NVM subsystem does not indicate a critical warning for the corresponding bit.

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Table 35: Subsystem Management Data (SMD) Structure (Continued)

Address	#Bytes	Value	Byte Offset	Description
0x6A (7-bit)	1	Variable	3	**Composite Temperature (CTemp):** Indicates the current temperature in degrees Celsius. If a temperature value is reported, it should be the same temperature as the composite temperature from the SMART log of hottest controller in the NVM subsystem. The reported temperature range is vendor specific, and shall not exceed the range –60 to +127°C. The 8-bit format of the data is shown below. This field should not report a temperature that is older than 5 seconds. If recent data is not available, the management endpoint should indicate a value of 80h for this field. 00h-7Eh: Temperature is measured in degrees Celcius (0°C to 126°C). 7Fh: 127° or higher. 80h: No temperature data or temperature data is more than 5 seconds old. 81h: Temperature sensor failure. 82h-C3h: Reserved. C4: Temperature is -60°C or lower. C5-FFh: Temperature measured in degrees Celsius is represented in two's complement (–1°C to -59°C).
	1	Variable	4	**Percentage Drive Life Used (PDLU):** Contains a vendor specific estimate of the percentage of NVM subsystem NVM life used based on the actual usage and the manufacturer's prediction of NVM life. A value of 100 indicates that the estimated endurance of the NVM in the NVM subsystem has been consumed, but may not indicate an NVM subsystem failure. The value is allowed to exceed 100. Percentages greater than 254 shall be represented as 255. This value should be updated once per power-on hour and equal the percentage used value in the NVMe SMART health log page.
	2	0	5-6	Reserved.
	1	Variable	7	**PEC:** An 8-bit CRC calculated over the slave address, command code, second slave address and returned data. The algorithm is defined in the SMBus specification.
	1	16h	8	**Length of Identification:** Indicates number of additional bytes to read before encountering PEC.
	2	13h	9	**Vendor ID:** The 2-byte vendor ID, assigned by the PCI SIG. Note the MSB is transmitted first.
		44h	10	
	20	Variable	11-30	**Serial Number:** 20 characters that match the serial number in the NVMe identify controller command response. Note the first character is transmitted first.
	1	Variable	31	**PEC:** An 8-bit CRC calculated over the slave address, command code, second slave address and returned data. The algorithm is defined in the SMBus specification.

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Interface Connectors

U.3 Enterprise PCIe

Figure 3: Interface Connections – U.3 Enterprise PCIe (SFF-8639)

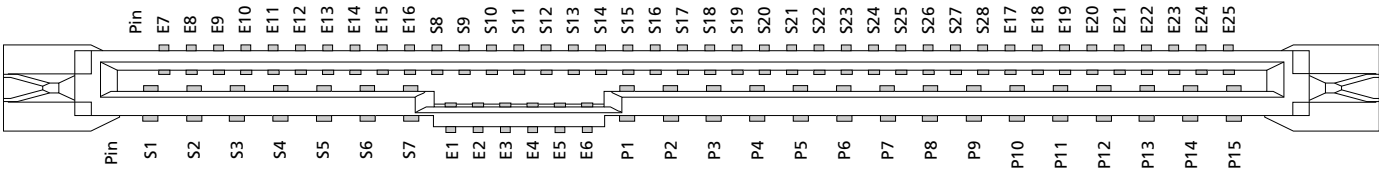

Table 36: Signal Assignments – U.3 Enterprise PCIe (SFF-8639)

Top Side			Bottom Side		
Pin #	**Signal Name**	**Description**	**Pin #**	**Signal Name**	**Description**
S1	GND	Ground	E7	RefClk0+	PCIe REFCLK+
S2	PETp0	PCIe TX+ Lane 0	E8	RefClk0-	PCIe REFCLK-
S3	PETn0	PCIe TX- Lane 0	E9	GND	Ground
S4	GND	Ground	E10	–	–
S5	PERn0	PCIe RX- Lane 0	E11	–	–
S6	PERp0	PCEI RX+ Lane 0	E12	GND	Ground
S7	GND	Ground	E13	–	–
E1	RefClk1+	No connect	E14	–	–
E2	RefClk1-	No connect	E15	GND	Ground
E3	3.3Vaux	+3.3V	E16	HPT1	No connect
E4	ePERst1#	No connect	S8	GND	Ground
E5	ePERst0#	PERST#	S9	PETp1	PCIe TX+ Lane 1
E6	IfDet2#	Ground	S10	PETn1	PCIe TX- Lane 1
P1	WAKE#	No connect	S11	GND	Ground
P2	–	–	S12	PERn1	PCIe RX- Lane 1
P3	PWRDIS	Power_Disable	S13	PERp1	PCIe RX+ Lane 1
P4	IfDet#	Ground	S14	GND	Ground
P5	GND	Ground	S15	HPT0	HPT0
P6	GND	Ground	S16	GND	Ground
P7	5V	No connect	S17	PETp2	PCIe TX+ Lane 2
P8	5V	No connect	S18	PETn2	PCIe TX- Lane 2
P9	5V	No connect	S19	GND	Ground
P10	PRSNT#	No connect	S20	PERn2	PCIe RX- Lane 2
P11	Activity	Drive activity signal	S21	PERp2	PCIe RX+ Lane 2
P12	GND	Ground	S22	GND	Ground
P13	12V	No connect	S23	PETp3	PCIe TX+ Lane 3
P14	12V	+12.0V	S24	PETn3	PCIe TX- Lane 3
P15	12V	+12.0V	S25	GND	Ground

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Table 36: Signal Assignments – U.3 Enterprise PCIe (SFF-8639)

Top Side			Bottom Side		
Pin #	**Signal Name**	**Description**	**Pin #**	**Signal Name**	**Description**
–	–	–	S26	PERn3	PCIe RX- Lane 3
–	–	–	S27	PERp3	PCIe RX+ Lane 3
–	–	–	S28	GND	Ground
–	–	–	E17	–	–
–	–	–	E18	–	–
–	–	–	E19	GND	Ground
–	–	–	E20	–	–
–	–	–	E21	–	–
–	–	–	E22	GND	Ground
–	–	–	E23	SMClk	SMBus clock
–	–	–	E24	SMDat	SMBus data
–	–	–	E25	DualPortEn#	DualPortEn#

M.2 Type 2280 and 22110

Figure 4: Interface Connections – M.2 Type 2280 and 22110

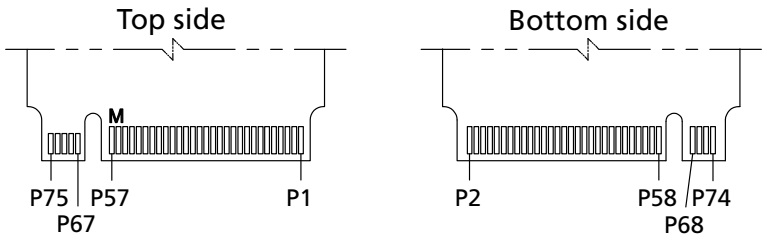

Table 37: Signal Assignments – M.2 Type 2280 and 22110

Top Side			Bottom Side		
Pin #	**Signal Name**	**Description**	**Pin #**	**Signal Name**	**Description**
1	GND	Ground	2	3V3	+3.3V
3	GND	Ground	4	3V3	+3.3V
5	PETn3	PCIe TX– Lane 3	6	PWRDIS	Power Disable
7	PETp3	PCIe TX+ Lane 3	8	NC8	No connect
9	GND	Ground	10	DAS/DSS#	Drive activity signal
11	PERn3	PCIe RX– Lane 3	12	3V3	+3.3V
13	PERp3	PCIe RX+ Lane 3	14	3V3	+3.3V
15	GND	Ground	16	3V3	+3.3V
17	PETn2	PCIe TX– Lane 2	18	3V3	+3.3V
19	PETp2	PCIe TX+ Lane 2	20	NC20	No connect
21	GND	Ground	22	NC22	No connect
23	PERn2	PCIe RX– Lane 2	24	NC24	No connect

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Table 37: Signal Assignments – M.2 Type 2280 and 22110

Top Side			Bottom Side		
Pin #	**Signal Name**	**Description**	**Pin #**	**Signal Name**	**Description**
25	PERp2	PCIe RX+ Lane 2	26	NC26	No connect
27	GND	Ground	28	NC28	No connect
29	PETn1	PCIe TX– Lane 1	30	NC30	No connect
31	PETp1	PCIe TX+ Lane 1	32	NC32	No connect
33	GND	Ground	34	NC34	No connect
35	PERn1	PCIe RX– Lane 1	36	NC36	No connect
37	PERp1	PCIe RX+ Lane 1	38	NC38	No connect
39	GND	Ground	40	SMClk	SMBus Clock
41	PETn0	PCIe TX– Lane 0	42	SMDat	SMBus Data
43	PETp0	PCIe TX+ Lane 0	44	NC44	No connect
45	GND	Ground	46	NC46	No connect
47	PERn0	PCIe RX– Lane 0	48	NC48	No connect
49	PERp0	PCIe RX+ Lane 0	50	PERST#	PERST#
51	GND	Ground	52	CLKREQ#	CLKREQ#
53	REFCLKn	PCIe REFCLK–	54	PEWAKE#	No connect
55	REFCLKp	PCIe REFCLK+	56	MFG1	Reserved
57	GND	Ground	58	MFG2	Reserved
Mechanical M Key			**Mechanical M Key**		
67	NC67	No Connect	68	SUSCLK	No connect
69	PEDET	No Connect	70	3V3	+3.3V
71	GND	Ground	72	3V3	+3.3V
73	GND	Ground	74	3V3	+3.3V
75	GND	Ground	–	–	–

EDSFF

Figure 5: Interface Connections – EDSFF

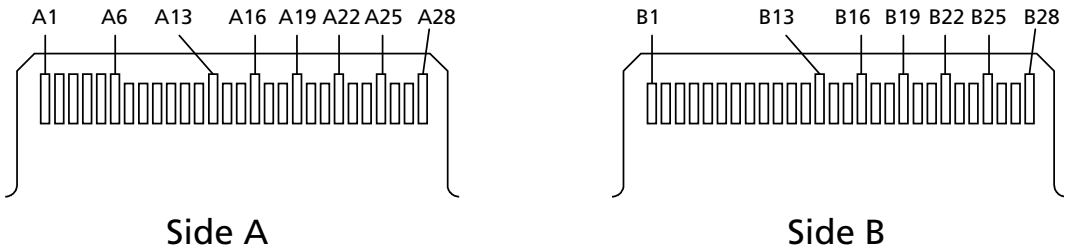

Table 38: Signal Assignments – EDSFF

Side A			Side B		
Pin #	**Signal Name**	**Description**	**Description**	**Signal Name**	**Pin #**
A1	GND	Ground	+12.0V	12V	B1

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Table 38: Signal Assignments – EDSFF

Side A			Side B		
Pin #	**Signal Name**	**Description**	**Description**	**Signal Name**	**Pin #**
A2	GND	Ground	+12.0V	12V	B2
A3	GND	Ground	+12.0V	12V	B3
A4	GND	Ground	+12.0V	12V	B4
A5	GND	Ground	+12.0V	12V	B5
A6	GND	Ground	+12.0V	12V	B6
A7	SMBCLK	SMBus Clock	No connect	MFG	B7
A8	SMBDAT	SMBus Data	No connect	RFU	B8
A9	SMBRST#	SMBus Reset	No connect	DUALPORTEN#	B9
A10	LED#/DAS	Data activity signal	PERST#	PERST0#	B10
A11	PERST1#/CLKREQ#	No connect	+3.3V	3.3Vaux	B11
A12	PRSNT0#	No connect	12.0V_Disable	PWRDIS	B12
A13	GND	Ground	Ground	GND	B13
A14	REFCLKn1	No connect	PCIe Refclk-	REFCLKn0	B14
A15	REFCLKp1	No connect	PCIe Refclk+	REFCLKp0	B15
A16	GND	Ground	Ground	GND	B16
A17	PERn0	PCIe RX- Lane 0	PCIe TX- Lane 0	PETn0	B17
A18	PERp0	PCIe RX+ Lane 0	PCIe TX+ Lane 0	PETp0	B18
A19	GND	Ground	Ground	GND	B19
A20	PERn1	PCIe RX- Lane 1	PCIe TX- Lane 1	PETn1	B20
A21	PERp1	PCIe RX+ Lane 1	PCIe TX+ Lane 1	PETp1	B21
A22	GND	Ground	Ground	GND	B22
A23	PERn2	PCIe RX- Lane 2	PCIe TX- Lane 2	PETn2	B23
A24	PERp2	PCIe RX+ Lane 2	PCIe TX+ Lane 2	PETp2	B24
A25	GND	Ground	Ground	GND	B25
A26	PERn3	PCIe RX- Lane 3	PCIe TX- Lane 3	PETn3	B26
A27	PERp3	PCIe RX+ Lane 3	PCIe TX+ Lane 3	PETp3	B27
A28	GND	Ground	Ground	GND	B28

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PCI Express Configuration Space Headers

Table 39: 7400 PRO PCIe Configuration Space Header

Bits 31:24	Bits 23:16	Bits 15:8	Bits 7:0
Device ID (DID) = 51C0h		Vendor ID (VID) = 1344h	
		Command register	
		Status register	
			Revision ID (RID) = 0x01

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Table 39: 7400 PRO PCIe Configuration Space Header (Continued)

Bits 31:24	Bits 23:16	Bits 15:8	Bits 7:0
	Base class code (BCC) = 0x01	Subclass code (SCC) = 0x08	Programming interface (PI) = 0x02
Memory address register base address lower (BAR0)			
Memory address register base address upper (BAR1)			
Index/Data pair register base address (BAR2)			
Reserved (BAR3)			
Vendor specific (BAR4)			
Vendor specific (BAR5)			
Subsystem ID (SSID) = 1100h (M.2 480GB)		Subsystem vendor ID (SSVID) = 1344h	
Subsystem ID (SSID) = 2100h (M.2 960GB)			
Subsystem ID (SSID) = 2B00h (M.2 1920GB)			
Subsystem ID (SSID) = 3E00h (M.2 3840GB)			
Subsystem ID (SSID) = 1000h (U.3 480GB)			
Subsystem ID (SSID) = 2000h (U.3 960GB)			
Subsystem ID (SSID) = 3000h (U.3 1920GB)			
Subsystem ID (SSID) = 4000h (U.3 3840GB)			
Subsystem ID (SSID) = 5000h (U.3 7680GB)			
Subsystem ID (SSID) = 0x1600 (E1.S 480GB)			
Subsystem ID (SSID) = 2600h (E1.S 960GB)			
Subsystem ID (SSID) = 2D00h (E1.S 1920GB)			
Subsystem ID (SSID) = 3F00h (E1.S 3840GB)			

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Table 40: 7400 MAX PCIe Configuration Space Header

Bits 31:24	Bits 23:16	Bits 15:8	Bits 7:0
Device ID (DID) = 51C1h		Vendor ID (VID) = 1344h	
		Command register	
		Status register	
			Revision ID (RID) = 0x01
	Base class code	Subclass code	Programming
Memory address register base address lower (BAR0)			
Memory address register base address upper (BAR1)			
Index/Data pair register base address (BAR2)			
Reserved (BAR3)			
Vendor specific (BAR4)			
Vendor specific (BAR5)			
Subsystem ID (SSID) = 1100h (M.2 400GB)		Subsystem vendor ID (SSVID) = 1344h	
Subsystem ID (SSID) = 2100h (M.2 800GB)			
Subsystem ID (SSID) = 2B00h (M.2 1600GB)			
Subsystem ID (SSID) = 3E00h (M.2 3200GB)			
Subsystem ID (SSID) = 1000h (U.3 400GB)			
Subsystem ID (SSID) = 2000h (U.3 800GB)			
Subsystem ID (SSID) = 3000h (U.3 1600GB)			
Subsystem ID (SSID) = 4000h (U.3 3200GB)			
Subsystem ID (SSID) = 5000h (U.3 6400GB)			
Subsystem ID (SSID) = 0x1600 (E1.S 400GB)			
Subsystem ID (SSID) = 2600h (E1.S 800GB)			
Subsystem ID (SSID) = 2D00h (E1.S 1600GB)			
Subsystem ID (SSID) = 3F00h (E1.S 3200GB)			

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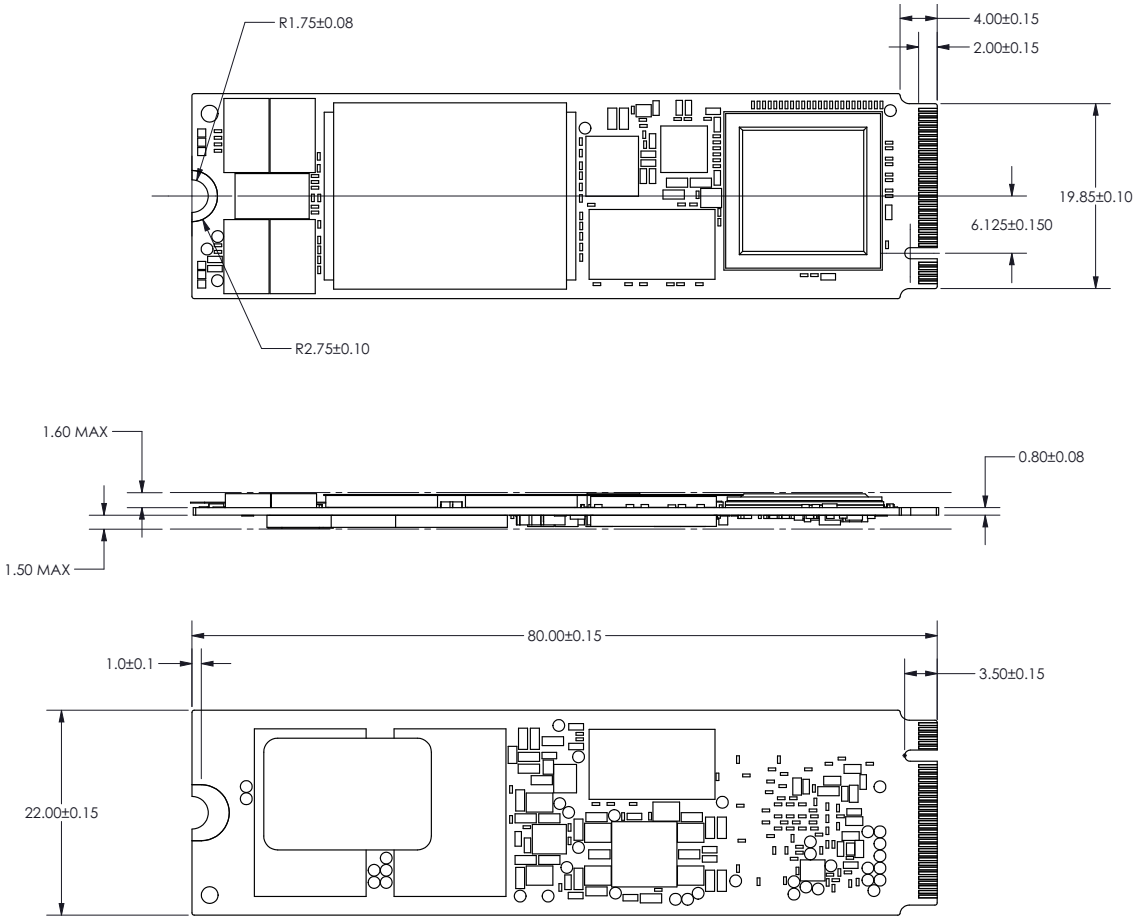
Physical Configuration

M.2 Type 2280 and 22110

M.2 Type 2280 product mass: less than 10 grams

M.2 Type 22110 product mass: less than 14 grams

Figure 6: M.2 Type 2280 Nominal Dimensions



Note: 1. All dimensions are in millimeters.

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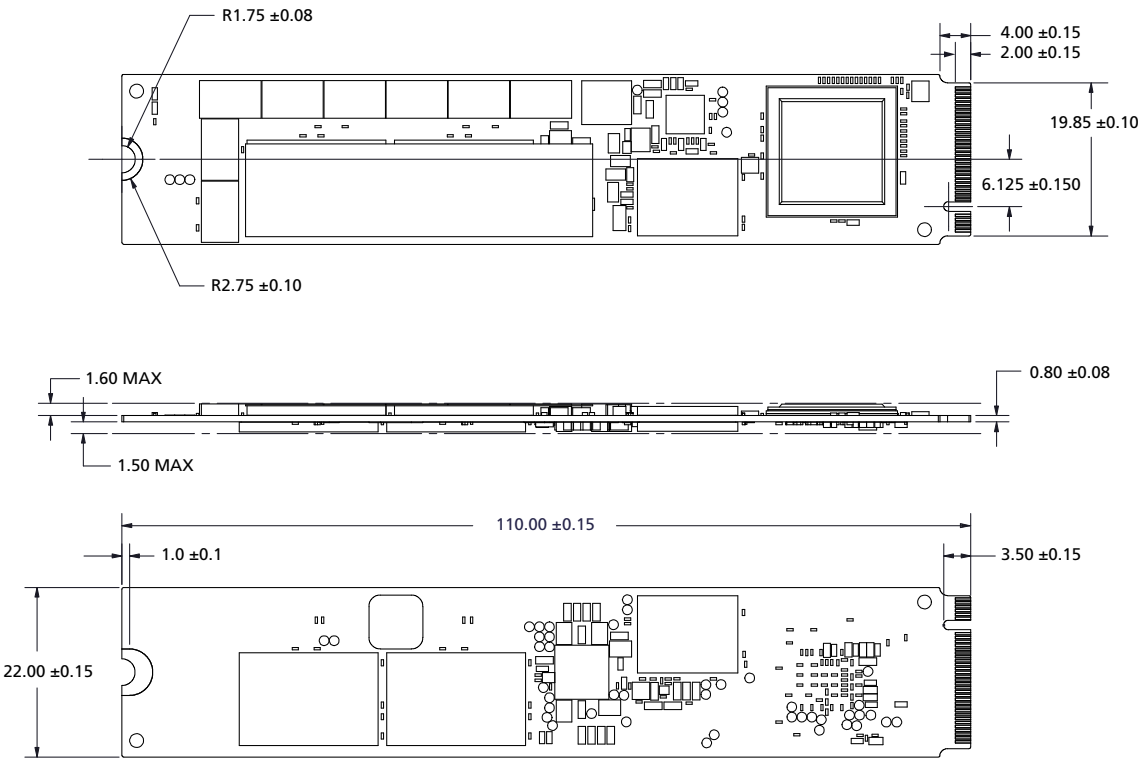
Figure 7: M.2 Type 22110 Nominal Dimensions



Note: 1. All dimensions are in millimeters.

Table 41: M.2 Type 2280 and 22110 Maximum Dimensions

Capacity (GB)	Width	Length	Height	Unit
400	22.00	80.00/110.00	3.9	mm
480				
800				
960				
1600	22.00	110.00	3.9	mm
1920				
3200				
3840				

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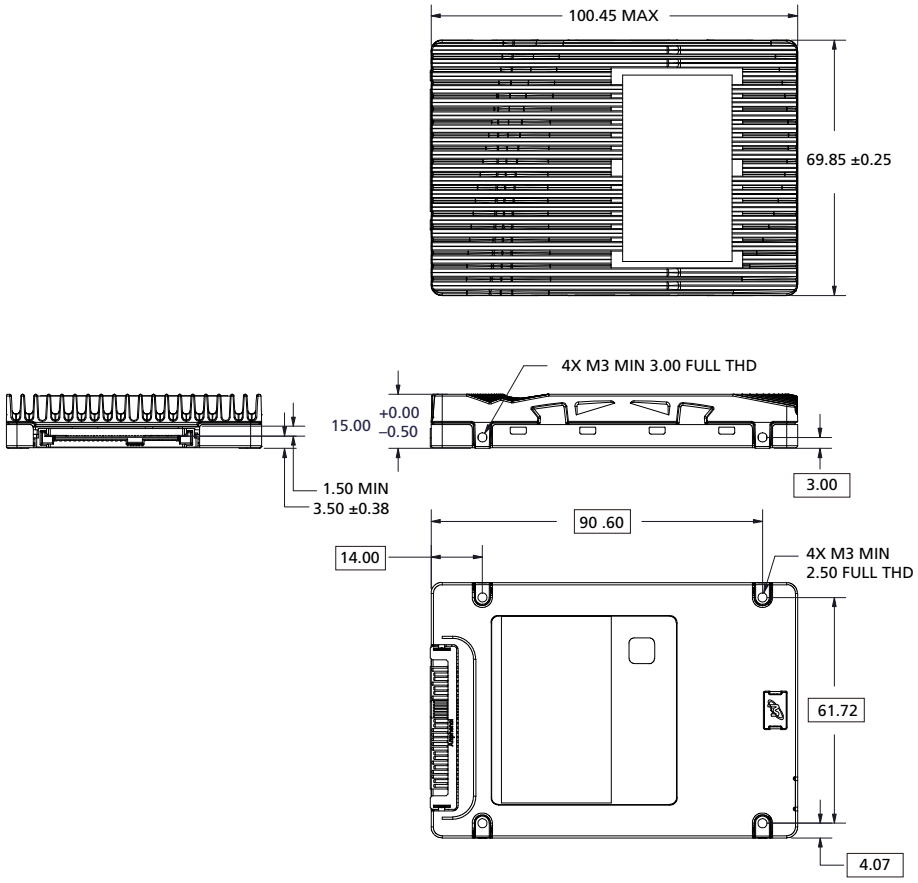
U.3 Enterprise PCIe (SFF - 8201 and SFF - 8223)

Product mass: less than 90 grams.

Figure 8: U.3 15mm Nominal Dimensions



Note: 1. All dimensions are in millimeters.

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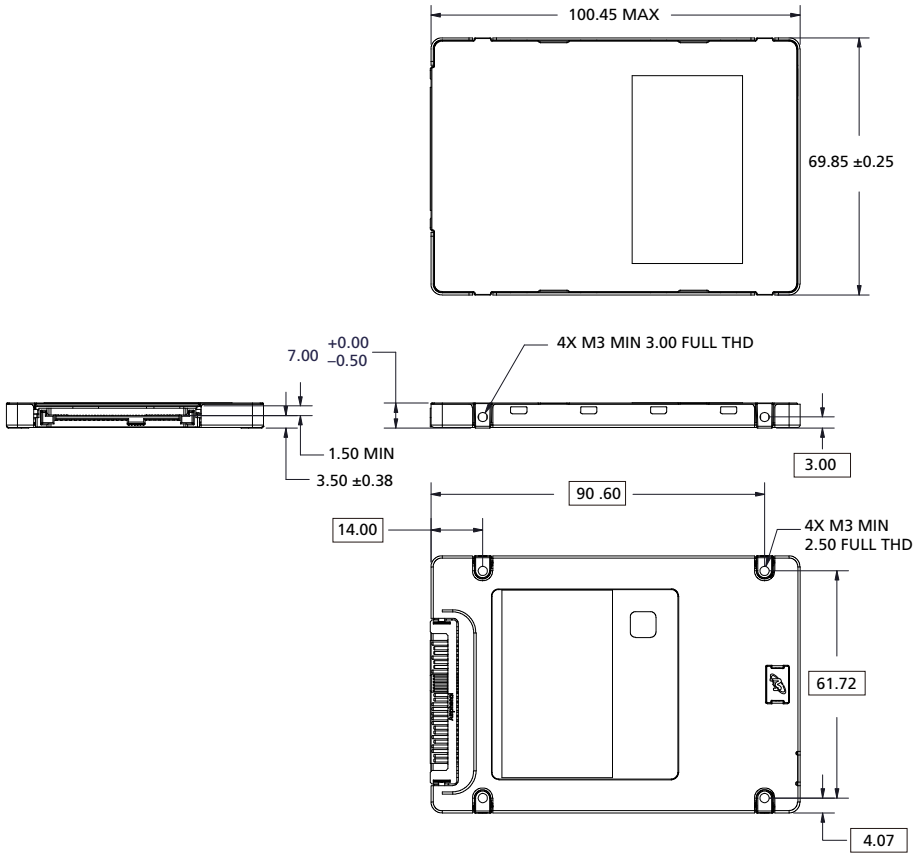
Figure 9: U.3 7mm Nominal Dimensions



Note: 1. All dimensions are in millimeters.

Table 42: U.3 Enterprise PCIe Maximum Dimensions

Capacity (GB)	Width	Length	Height	Unit
800	70.10	100.45	7.00/15.00	mm
960				
1600				
1920				
3200				
3840				
6400				
7680				

Note: 1. Dimension values per SFF - 8201, Revision 3.4 and SFF - 8223 Revision 2.7.

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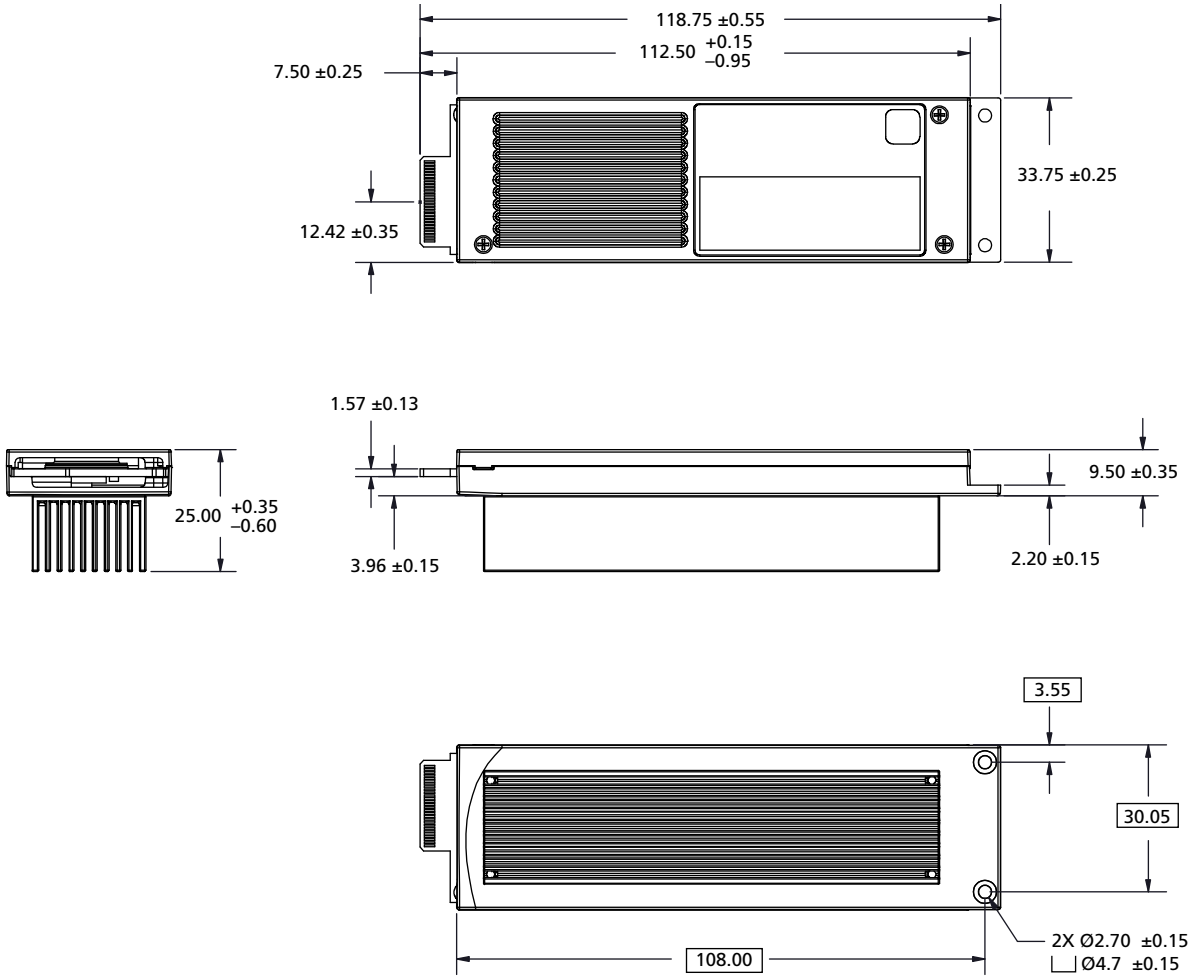
E1.S Enterprise PCIe x4

Product mass: less than 130g/100g/26g grams (E1.S 15mm/5.9mm).

Figure 10: E1.S 25mm Nominal Dimensions



Note: 1. All dimensions are in millimeters.

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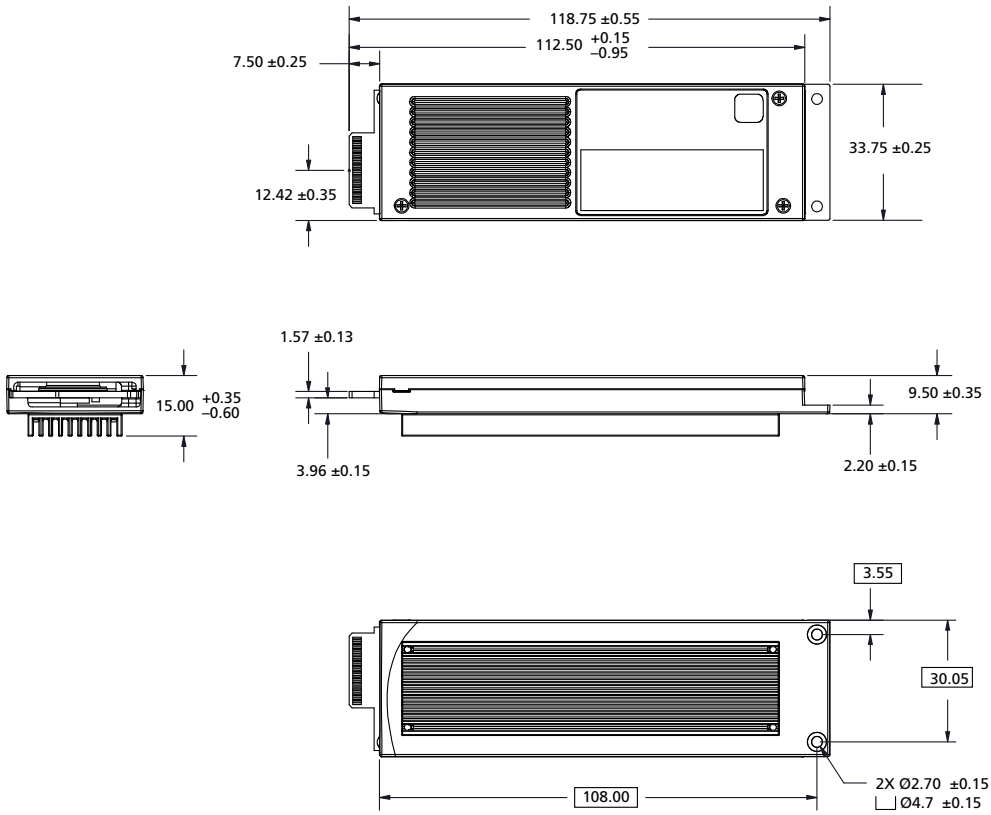
Figure 11: E1.S 15mm Nominal Dimensions



Note: 1. All dimensions are in millimeters.

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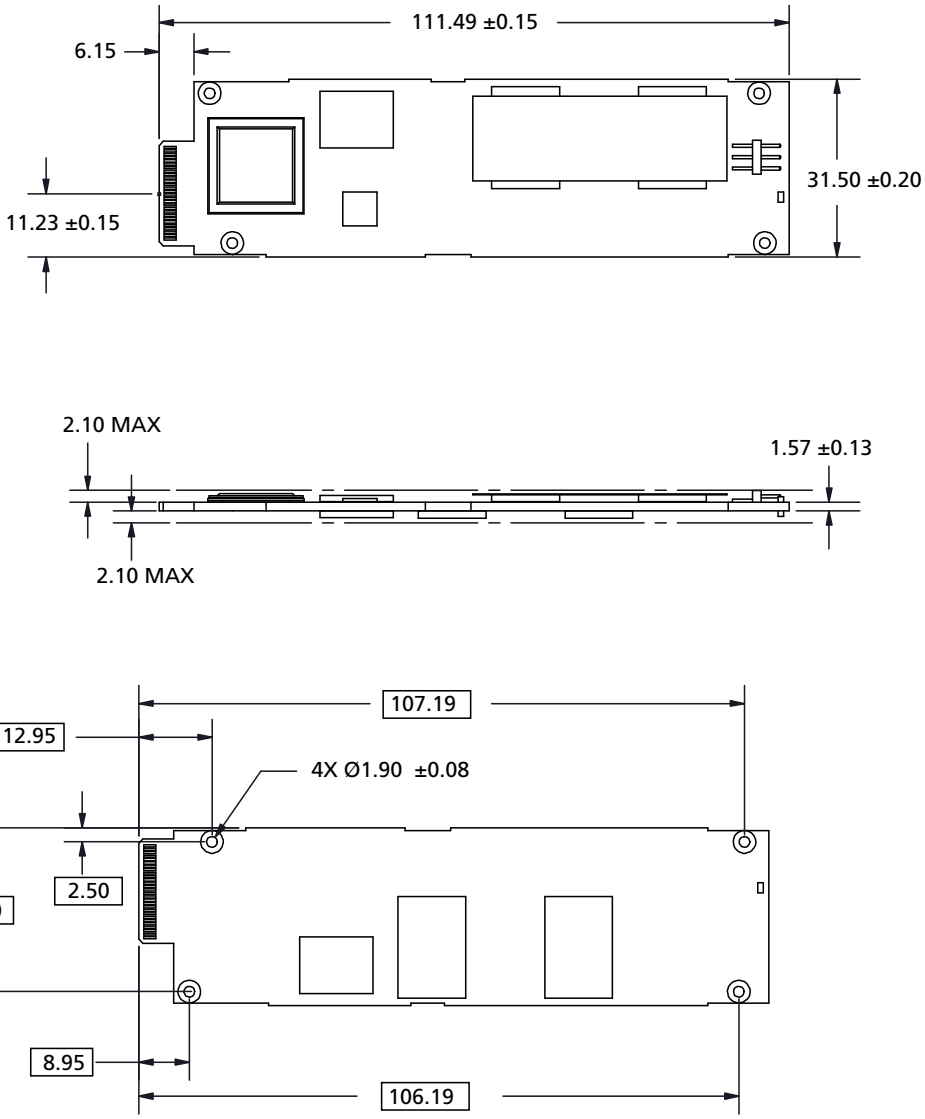
Figure 12: E1.S 5.9mm Nominal Dimensions



Note: 1. All dimensions are in millimeters.

Table 43: E1.S Enterprise PCIe x4 Maximum Dimensions

Capacity (GB)	Width	Length	Height	Unit
800	33.75	118.75	15.00	mm
960				
1600				
1920				
3200				
3840				

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Table 43: E1.S Enterprise PCIe x4 Maximum Dimensions (Continued)

Capacity (GB)	Width	Length	Height	Unit
800	31.50	111.50	5.90	mm
960				
1600				
1920				
3200				
3840				

Note: 1. Dimension values per SFF-TA-1006 REVISION 1.4.

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Compliance

Micron SSDs comply with the following:

- Micron Green Standard
- Built with sulfur-resistant resistors
- CE (Europe): EN55032, EN55024 Class B, RoHS
- FCC: CFR Title 47, Part 15, Class B
- UL/cUL: approval to UL-60950-1, 2nd Edition, IEC 60950-1:2005 (2nd Edition); EN 60950-1 (2006) + A11:2009+ A1:2010 + A12:2011 + A2:2013
- BSMI (Taiwan): approval to CNS 13438, Class B, CNS 15663
- RCM (Australia, New Zealand): AS/NZS CISPR32 Class B
- KC RRL (Korea): approval to KN32 Class B, KN 35 Class B

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- W.E.E.E.: Compliance with EU WEEE directive 2012/19/EC. Additional obligations may apply to customers who place these products in the markets where WEEE is enforced.
- TUV (Germany): approval to IEC60950/EN60950
- V_{CCI} (Japan): 2015-04 Class B

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的としていますが、この装置がラジオやテレビジョン受信機に近接して使用されると、
受信障害を引き起こすことがあります。
取扱説明書に従って正しい取り扱いをして下さい。
VCCIーB

- IC (Canada): ICES-003 Class B
  - This Class B digital apparatus complies with Canadian ICES-003.
  - Cet appareil numérique de la classe B est conforme à la norme NMB-003 du Canada.
- Morocco: EN55032, EN55024 Class B
- UkrSEPRO (Ukraine): EN55032 Class B, IEC60950/EN60950, RoHS (Resolution 2017 No. 139)

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FCC Rules

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

References

- NVM Express, Revision 1.4
- PCI Express Base Specification, Revision 4.0
- PCI Express Card Electromechanical (CEM), Revision 4.0
- PCI Express M.2 Electromechanical Specification , Revision 1.1
- Enterprise SSD Form Factor Version 1.0a
- NVM Express Management Interface, Revision 1.1
- JESD2 18A Solid State Drive (SSD) Requirements and Endurance Test Method
- Telcordia Reliability Prediction Procedure for Electronic Equipment SR-332
- SFF-8201 Revision 3.3
- SFF-TA-1002 Protocol Agnostic Multi-Lane High Speed Connector (EDSFF) rev. 1.0b
- SFF-TA-1006 EDSFF 1U Short Form Factor rev. 1.1
- SFF-TA-1009 EDSFF Pin and Signal Specification rev. 2.0
- TCG Storage Architecture Core Specification Version 2.01 Revision 1.00
- TCG Storage Interface Interactions Specification (SIIS) Version 1.08 Revision 1.00
- TCG Storage Security Subsystem Class: Opal Specification Version 2.01 Revision 1.00
- SFF-8201 Rev 3.4
- SFF-8223 Rev 2.7

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Revision History

Rev. B – 06/2021

- Updated Micron part numbers
- Updated Performance tables

Rev. A – 02/2021

- Initial release

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