SAMSUNG

Rev. 1.1, Dec. 2021

MZWJJ800HMGQ-00007

MZWJJ1T6HMGG-00007

MZWJJ3T2HMHN-00007

SAMSUNG SSD SZ1735

Specification (PCIe® NVMe™ 2.5")

Datasheet

SAMSUNG ELECTRONICS RESERVES THE RIGHT TO CHANGE PRODUCTS, INFORMATION AND SPECIFICATIONS WITHOUT NOTICE.

Products and specifications discussed herein are for reference purposes only. All information discussed herein is provided on an "AS IS" basis, without warranties of any kind.

This document and all information discussed herein remain the sole and exclusive property of Samsung Electronics. No license of any patent, copyright, mask work, trademark or any other intellectual property right is granted by one party to the other party under this document, by implication, estoppel or otherwise.

Samsung products are not intended for use in life support, critical care, medical, safety equipment, or similar applications where product failure could result in loss of life or personal or physical harm, or any military or defense application, or any governmental procurement to which special terms or provisions may apply.

For updates or additional information about Samsung products, contact your nearest Samsung office.

All brand names, trademarks and registered trademarks belong to their respective owners.

IF THERE IS ANY OTHER OPERATION TO IMPLEMENT IN ADDITION TO SPECIFICATION IN THE DATASHEET OR JEDEC STANDARD, PLEASE CONTACT EACH BRANCH OFFICE OR HEADQUARTERS OF SAMSUNG ELECTRONICS.

CONFIDENTIAL

Revision History

Revision No.	History	Draft Date	Remark	Editor	Review By
0.1	1. Initial issue	July. 13, 2018	Target	H.B. SON	H.B. SON
1.0	2. Initial Issue	Mar. 29. 2019	Final	J.H.KIM	J.H.KIM
1.1	1. Typo corrected	Dec. 27. 2021	Final	J.H.KIM	J.H.KIM

Part Number	Capacity[1)]	LBA (512 Bytes size)
MZWJJ800HMGQ - 00007	800GB	1,562,824,368
MZWJJ1T6HMGG - 00007	1.6TB	3,125,627,567
MZWJJ3T2HMHN - 00007	3.2TB	6,251,233,967

NAND

- Z-NAND Flash Memory

FEATURES

- PCI Express Gen3
  - Single port x4 lanes
  - Dual port x2 lanes
- Enhanced Power-Loss Data Protection
- LDPC ECC
- End-to-End Data Protection
- Support Hot Plug/Removal
- Support up to 128 I/O Queues per Port
- Support Deallocate (a.k.a. TRIM) Command
- Support PCI Express AER (Advanced Error Reporting)
- Support 129 vectors for MSI-X
- Support SSD Enhanced S.M.A.R.T. Feature Set
- Hardware based AES-XTS 256-bit Encryption Engine
- Static and Dynamic Wear Leveling
- Support UEFI Expansion ROM
- Support SFF-8639 SMBus

DRIVE CONFIGURATION

• Form Factor	SFF-8639 2.5-inch
• Interface	PCI Express Gen3 x4
• Bytes per Sector	512, 520, 4096, 4160 Bytes

PERFORMANCE SPECIFICATIONS[2)]

• Data Transfer Rate[2] (128KB data size)	
- Sequential Read[3]	Up to 3,200 MB/s
- Sequential Write[3]	Up to 3,200 MB/s
• Data I/O Speed[2] (4KB data size, Sustained)	
- Random Read	Up to 800K IOPS
- Random Write	Up to 250K IOPS
• Latency (Sustained random workload)	
- Read (typical)[4]	20 us
- Read (best)[4]	12 us
- Write (typical)[5]	20 us
-Drive Ready Time (typical)	2 sec
• Quality of service	
- Read/Write (99%)	20/20 us
• Performance Consistency	
- Read/Write (99.9%)	Up to 98/95%

COMPLIANCE

- PCI Express Base Specification Rev. 3.0
- NVM Express Specification Rev. 1.2
- Enterprise SSD Form Factor Ver. 1.0a

CERTIFICATIONS AND DEDARATIONS

- c-UL-us, TUV-GS, CB, CE, BSMI, KC, Morocco, VCCI, RCM, FCC, IC

PRODUCT ECOLOGICAL COMPLIANCE

- RoHS

RELIABILITY SPECIFICATIONS

• Uncorrectable Bit Error Rate	1 sector per 10^{17} bits read
• MTBF	2,000,000 hours
• Power on Cycles (Ambient)	20,000
• Component Design Life	5 years
• Endurance	30 DWPD
• TBW (@4KB Random Write)	
- 800GB	43.8 PB
- 1.6TB	87.6 PB
- 3.2TB	175.2 PB
• Data Retention	3 months

ENVIRONMENTAL SPECIFICATIONS

• Temperature, Ambient (Ta [6])	
- Operating	0 ~ 55 °C
- Non-operating	-40 ~ 85 °C
• Humidity (Non-operating)	5 ~ 95%
• Shock	1,500 G / 0.5msec
• Vibration	
- Sweep Sinusoidal	20 Gpeak, 10 ~ 2000Hz

POWER REQUIREMENTS

• Supply Voltage / Tolerance	12V±10%
• Active[7] (max. RMS)	12 W
• Idle (typ.)	6 W

PHYSICAL DIMENSION

• Width	69.85 ± 0.25 mm
• Length	100.20 ± 0.25 mm
• Height	14.80 ± 0.20 mm
• Weight	Up to 190 g

OPERATING SYSTEMS

Windows Server 2008 R2 64-bit
Windows Server 2012 64-bit
Windows Server 2012 R2 64-bit
RHEL 6.4 (Kernel 2.6.32)
RHEL 6.5 (Kernel 2.6.32)
RHEL 6.6 (Kernel 2.6.32)
RHEL 7 (Kernel 3.10.0)
RHEL 7.1 (Kernel 3.10.0)
SLES 11 SP3 (Kernel 3.0.13)
SLES 12 (Kernel 3.12.28)

NOTE: Specifications are subject to change without notice.

1) 1MB = 1,000,000 Bytes, 1GB = 1,000,000,000 Bytes, unformatted Capacity. User accessible capacity may vary depending on operating environment and formatting.
2) Based on PCI Express Gen3 x4, Random performance measured using FIO in CentOS 7.0 with queue depth 32 by 16 workers and Sequential performance with queue depth 32 by 16 worker. Actual performance may vary depending on use conditions and environment.
3) 1 MB/sec = 1,000,000 bytes/sec was used in sequential performance.
4) The read latency is measured by using FIO in CentOS 7.0 and 4KB transfer size with queue depth 1 on a random workload of sustained state.
5) The write latency is measured by using FIO in CentOS 7.0 and 4KB transfer size with queue depth 1 on a sequential workload of sustained state.
6) Ta is the ambient temperature with enough cooling airflow condition as 150LFM or faster.
7) Active power is measured using IOMeter2006 on Win Server 2012 R2.

Table Of Contents

1.0 INTRODUCTION

1.1 General Description

This document describes the specifications of the Samsung SSD SZ1735, which is a native-PCIe SSD for enterprise application.
The Samsung SSD SZ1735 presents outstanding performance with instant responsiveness to the host system, by applying the Peripheral Component Interconnect Express (PCIe) 3.0 interface standard, as well as highly efficient Non-Volatile Memory Express (NVMe) Protocol.
The Samsung SSD SZ1735 delivers wide bandwidth of 3200 MB/s for sequential read speed and 3200 MB/s for sequential write speed under up to 12W power. With the help of Toggle 2.0 NAND Flash interface, the Samsung SSD SZ1735 delivers Quality of Service(99%) of 100us for random 4KB read of 800KIOPS and 600us for random 4KB write of 250KIOPS in the sustained state.
By combining the enhanced reliability Samsung NAND Flash memory silicon with NAND Flash management technologies, the Samsung SSD SZ1735 delivers the extended endurance of up to 30 Drive Writes Per Day (DWPD) for 5 years, which is suitable for enterprise applications, in a HHHL form factor lineups: 800GB, 1.6TB, 3.2TB
In addition, the Samsung SSD SZ1735 supports Hot Plug insertion and removal feature by employing the efficient circuitry for Power Loss Protection (PLP). PLP solution can guarantee that data issued by the host system are written to the storage media without any loss in the event of sudden power off or sudden power failure.

1.2 Product List

[Table 1] Product List

Type	Capacity	Part Number
2.5-inch[1)]	800GB	MZWJJ800HMGQ-00007
2.5-inch	1.6TB	MZWJJ1T6HMGG-00007
2.5-inch	3.2TB	MZWJJ3T2HMHN-00007

NOTE:
1) SFF-8639 combo (SATA, SAS, PCIe) standard connector

1.3 Ordering Information

MZ X X X XXX X X XX

Samsung SSD

Interface/Form Factor
P: PCIe HHHL (Half-height Half-length)

Line-Up
J: Z-NAND

SSD CTRL
J: Eagle, S.LSI

SSD Capacity
800: 800GB
1T6: 1.6TB
3T2: 3.2TB

NAND Density
GQ: 51T HDP 4CE
GG: 512G ODP 2CE(FBI)
HN: 1T HDP 2CE(FBI)

Flash Generation
M: 1th Generation

NAND PKG
H: BGA (LF, HF)

2.0 PRODUCT SPECIFICATIONS

2.1 Capacity

[Table 2] User Capacity and Addressable Sectors

Capacity[2]	Max LBA[3]
800GB	1,562,824,368
1.6TB	3,125,627,567
3.2TB	6,251,233,967

NOTE:
1) Gigabyte (GB) = 1,000,000,000 Bytes, 1 Sector = 512Bytes
2) Capacity shown in Table 2 represents the total usable capacity of the SSD which may be less than the total physical capacity. A certain area in physical capacity, not in the area shown to the user, might be used for the purpose of NAND flash management.
3) Max. LBA shown in Table 2 represents the total user addressable sectors in LBA mode and calculated by IDEMA rule.

2.2 Performance

[Table 3] Sustained Random Read/Write Performance (IOPS)

Maximum Performance[1)]	Unit	800GB / 1.6TB / 3.2TB
Random 4KB Read	IOPS	800K
Random 4KB Write	IOPS	250K
Random 8KB Read	IOPS	400K
Random 8KB Write	IOPS	100K

NOTE:
1) Random performance in Table 3 was measured by using FIO in CentOS7.0 with queue depth 32 by 16 workers. Measurements were performed on a full Logical Block Address (LBA) span of the drive in sustained state. Actual performance may vary depending on use conditions and environment.

[Table 4] Sequential Read/Write Performance

Maximum Performance[1)]	Unit	800GB / 1.6TB / 3.2TB
Sequential 128KB Read[2)]	MB/s	3,200
Sequential 128KB Write[2)]	MB/s	3,200

NOTE:
1) Sequential performance in Table 4 was measured by using FIO in CentOS7.0 with queue depth 32 by 16 worker. Actual performance may vary depending on use conditions and environment.
2) 1 MB/sec = 1,000,000 bytes/sec was used in sequential performance.

2.3 Latency

[Table 5] Latency[1] (sustained state)

Queue Depth = 1	Unit	800GB / 1.6TB / 3.2TB
Random Read/Write2	us	20 / 20
Sequential Read/Write3	us	20 / 20
Drive Ready Time4	sec	2

NOTE:
1) Typical values.
2) The random read/write latency is measured by using FIO in CentOS7.0 and 4KB transfer size with queue depth 1 on a random workload of sustained state.
3) The sequential read/write latency is measured by using FIO in CentOS7.0 and 4KB transfer size with queue depth 1 on a sequential workload of sustained state.
4) The maximum taking time to be ready for receiving commands after power-up (CSTS.Ready=1). It is expected that I/O commands may not be completed at this point.

2.4 Quality of Service (QoS)

[Table 6] Quality of Service (QoS)

Quality of Service (99%)	Unit	800GB	1.6TB	3.2TB
Read(4KB) QD=1	us	20	20	20
Write(4KB) QD=1	us	29	20	20
Read(4KB) QD=32	us	100	100	100
Write(4KB) QD=32	us	600	600	600

Quality of Service (99.99%)	Unit	800GB	1.6TB	3.2TB
Read(4KB) QD=1	us	25	25	25
Write(4KB) QD=1	us	23	23	23
Read(4KB) QD=32	us	120	120	120
Write(4KB) QD=32	us	800	800	800

NOTE:
1) QoS is measured using FIO (99/99.99 %) with queue depth 1 and 32 on 4 KB random and write.
2) QoS is measured as the maximum round-trip time taken for 99 % of commands to host.
3) QoS is measured as the maximum round-trip time taken for 99.99 % of commands to host.

2.5 IOPS Consistency

[Table 7] IOPS Consistency

IOPS Consistency1, 2	Unit	800GB	1.6TB	3.2TB
Random Read (4 KB)	%	98	98	98
Random Write (4 KB)	%	95	95	95
Random Read (8 KB)	%	98	98	98
Random Write (8 KB)	%	95	95	95

NOTE:
1) IOPS consistency measured using FIO with queue depth 128.
2) IOPS Consistency (%) = (IOPS in the 99.9% slowest 1-second interval)/(average IOPS during the test).

2.6 Power

The Samsung SSD SZ1735 is implemented in standardized 2.5-inch form factor and gets primary 12V power as well as auxiliary 3.3V (3.3Vaux) power through the indicated pins (#P13~15 for 12V and #E3 for 3.3Vaux in SFF-8639 connector plug) from the host system.
For 12V and 3.3Vaux, the allowable voltage tolerance and noise level in SSD are described in chapter 2.6.1, the power consumption in 2.6.2 and the inrush current in 2.6.3.

2.6.1 Maximum Voltage Ratings (12V and 3.3Vaux)

[Table 8] Allowable Voltage Tolerance[1]

Operating Voltage	800GB/1.6TB/3.2TB
12V[2]	10%
12V Rise time (Max/Min)	50ms/1ms
12V Fall time (Max/Min)[4]	5s/1ms
12V Noise level	300 mV pp 10Hz – 100 KHz 50 mV pp 100KHz – 20 MHz
3.3Vaux[3]	10%
3.3Vaux Rise time (Max/Min)	50ms/1ms
3.3Vaux Fall time (Max/Min)[4]	5s/1ms
3.3Vaux Noise level	300 mV pp 10Hz – 100 KHz 50 mV pp 100KHz – 20 MHz

NOTE:
1) The components inside SSD were designed to endure the range of voltage fluctuations, which might be induced by the host system, in Table 8.
2) For 12V operating voltage, the minimum allowable is 10.8V and the maximum 13.2V.
3) For 3.3Vaux, the minimum allowable voltage is 2.97V and the maximum 3.63V.
4) Fall time needs to be equal or better than minimum in order to guarantee full functionality of enhanced power loss management.

2.6.2 Power Consumption (12V)

In enterprise server and storage system, the Samsung SSD SZ1735 is designed for the specific usage, which means that SSD will be always operated by the host system during the entire life. Hence, the Samsung SSD SZ1735 does not manage any low power modes except for the Active/Idle, Off mode.

[Table 9] Power Consumption (12V Supply Voltage)[1]

Power Mode		800GB/1.6TB/3.2TB
Active[2]	Read	11.5W
	Write	12W
Idle[3]		5W
Off		0W

NOTE:
1) Power consumption was measured in the 12V power pins (#P13~#P15) of the connector plug in SSD. The active and idle power is defined as the highest averaged power value, which is the maximum RMS average value over 100 ms duration.
2) The measurement condition for active power is assumed for 100% sequential read or write.
3) The idle state is defined as the state that the host system can issue any commands into SSD at any time.

2.7 Reliability

The reliability specification of the Samsung SSD SZ1735 follows JEDEC standard, which are included in JESD218A and JESD219A documents.

2.7.1 Mean Time Between Failures

By definition, Mean Time between Failures (MTBF) is the estimated time between failures occurring during SSD operation.

[Table 10] MTBF Specifications

Parameter	800GB/1.6TB/3.2TB
MTBF	2,000,000 Hours

2.7.2 Uncorrectable Bit Error Rate

By definition, Uncorrectable Bit Error Rate (UBER) is a metric for the rate of occurrence of data errors, equal to the number of data errors per bits read as specified in the JESD218 document of JEDEC standard.

[Table 11] UBER Specifications

Parameter	800GB/1.6TB/3.2TB
UBER	1 sector per 10^{17} bits read

NOTE:
1) For the enterprise application, JEDEC recommends that UBER shall be below 10^{-16}

2.7.3 Data Retention

By definition, data retention is the expected time period for retaining data in the SSD at the maximum rated endurance in power-off state as specified in the JESD218 document of JEDEC standard.

[Table 12] Data Retention

Parameter	800GB/1.6TB/3.2TB
Data Retention[1]	3 months

NOTE:
1) Data retention was measured by assuming that SSD reaches the maximum rated endurance at 40C in power-off state.

2.7.4 Endurance

By definition, the endurance of SSD in enterprise application is defined as the maximum number of drive writes per day that can meet the requirements specified in the JESD218 document of JEDEC standard.

[Table 13] Drive Write Per Day (DWPD)

Parameter	800GB/1.6TB/3.2TB

DWPD	30 drive writes per day over 5 years

[Table 14] Petabyte Written (PBW)

Parameter	Unit	800GB	1.6TB	3.2TB
PBW	PB	43.8	87.6	175.2

NOTE:
1) Relational formula between DWPD and PBW is like below:
PBW = DWPD x 365 x 5 x User capacity

2.8 Hot Plug Support

2.8.1 Power Loss Protection

By using internal back-up power technology, the Samsung SSD SZ1735 supports power loss protection (PLP) feature to guarantee the reliability of data requested by the host system. When power is unpredictably lost, SSD can detect automatically this abnormal situation and transfer all user data and meta-data cached in DRAM into the Flash media during any SSD operations.

2.8.2 Inrush Current Protection

When the Samsung SSD SZ1735 plugs in the backplane of host system, the significant amount of current is induced through 12V power rail. The Samsung SSD SZ1735 has protection circuitry including a set of resisters and capacitors to alleviate the impact by inrush current through 12V power.

[Table 15] Inrush Current

Inrush Current	800GB/1.6TB/3.2TB
12 V	1.5A[1)]

NOTE:
1) The measurement value of inrush current is also compatible with the standard specification of “Enterprise SSD Form Factor Version 1.0a” released by SSD Form Factor Working Group.

2.9 Environmental Specification

2.9.1 Temperature

[Table 16] Temperature

		800GB/1.6TB/3.2TB
Temperature[1)]	Operating	0 to 70℃
	Non-Operating[2)]	-40 to 85℃

NOTE:
1) Temperature of the hottest point on the case (Tc). The device will be working properly within the operating temperature range without deteriorating device long-term reliability and any throttling. Sufficient airflow would be recommended to be operated properly on any heavier workloads within device operating temperature.
2) Unbiased state

2.9.2 Humidity

[Table 17] Humidity

		800GB/1.6TB/3.2TB
Humidity[1]	Non-operating	5% to 95%

NOTE:
1) Humidity is measured in non-condensing state.

2.9.3 Shock and Vibration

[Table 18] Shock and Vibration

		800GB/1.6TB/3.2TB
Shock[1]	Non-operating	1,500G
Vibration[2]	Non-operating	20 Gpeak (10~2,000Hz, Sweep sine)

NOTE:
1) Shock specifications assume that SSD shall be mounted with screws when input vibration is applied. Vibration may be applied in 3 axes (x, y and z) with a half sine waveform of 0.5ms duration in non-operating condition.
2) Vibration specifications assume that SSD shall be mounted with screws when input vibration is applied. The input vibration may be applied in 3 axes (x, y and z) and lasts during 15 minutes per axis.

3.0 MECHANICAL SPECIFICATIONS

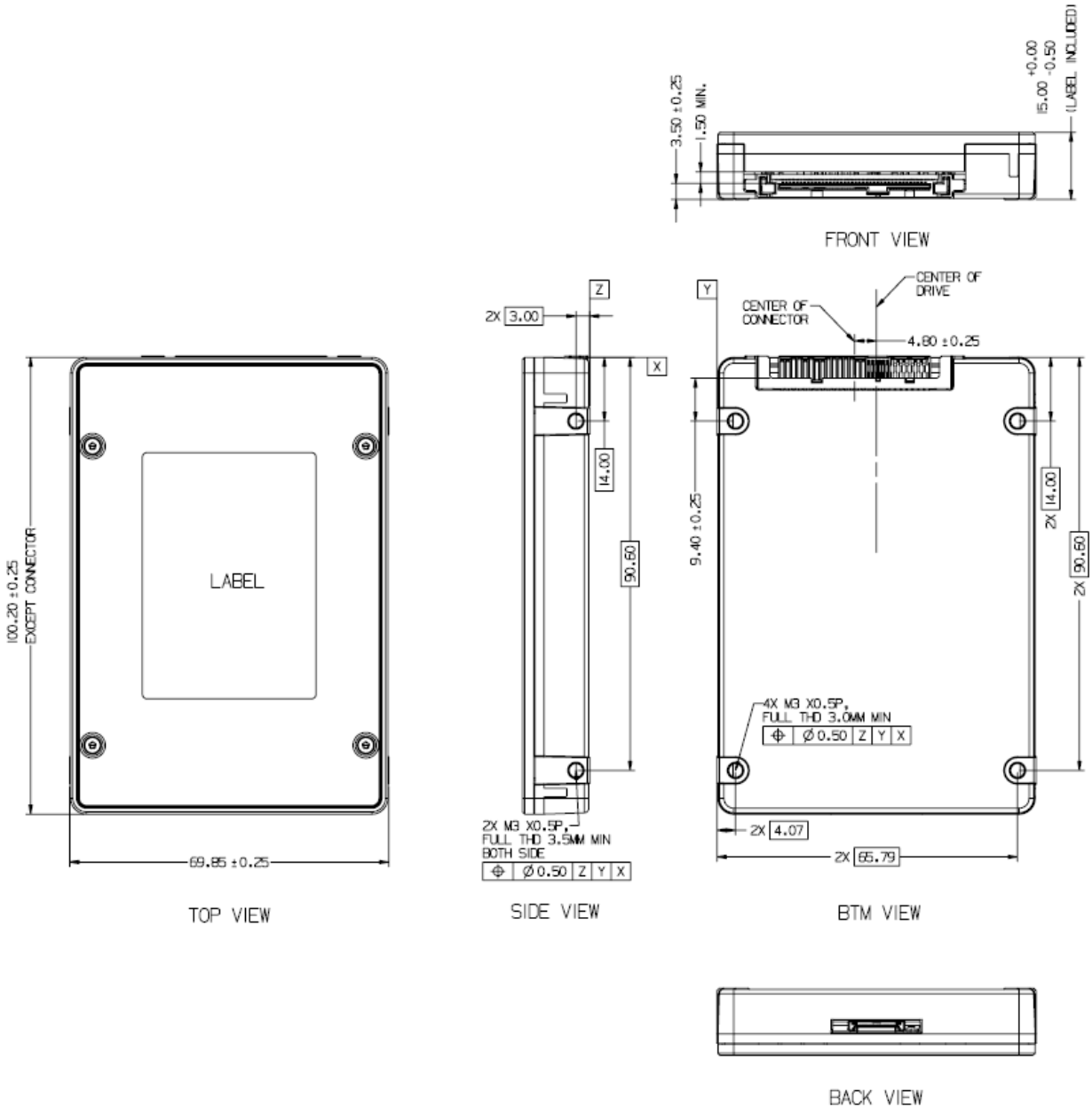
3.1 Physical Information

The physical case of the Samsung SSD SZ1735 in 2.5-inch form factor follows the standardized dimensions defined by SSD Form Factor Work Group.

[Table 19] Physical Dimensions and Weight

Parameter	Unit	800GB/1.6TB/3.2TB
Width	mm	69.85±0.25
Length	mm	100.20±0.25
Thickness	mm	14.80±0.20
Weight	g	Up to 190g

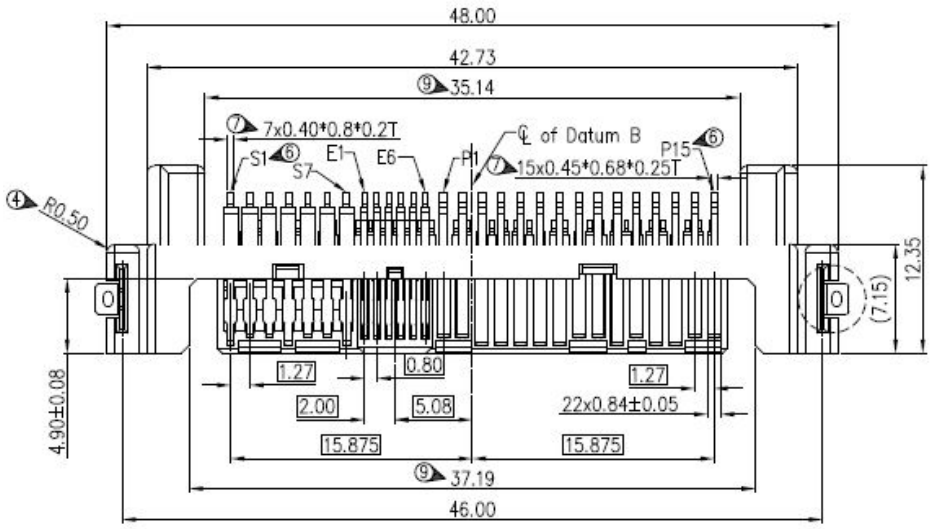
Figure 1. Mechanical Outline



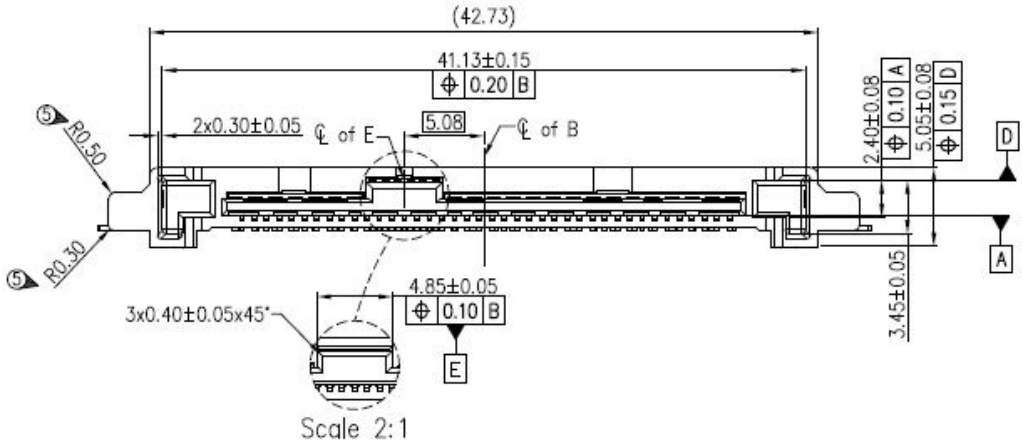
4.0 INTERFACE SPECIFICATION

The PCIe connector of SZ1735 is compliant with SFF-8639 standard specification.

4.1 Connector Dimensions



<Top View>



<Bottom View>

Figure 1. Layout of 2.5-inch Form Factor Connector Pins

4.2 Connector Pin Assignments

[Table 20] Certifications and Declarations

Pin #	Assignment	Description		Pin #	Assignment	Description
S1	Not Used	Float		E7	RefClk0+	PCIe Reference Clock + (primary port A)
S2	Not Used			E8	RefClk0-	PCIe Reference Clock - (primary port A)
S3	Not Used			E9	GND	Ground
S4	Not Used	Ground		E10	PETp0	PCIe Transmit+ (lane 0)
S5	Not Used			E11	PETn0	PCIe Transmit- (lane 0)
S6	Not Used			E12	GND	Ground
S7	Not Used	Ground		E13	PERn0	PCIe Receive- (lane 0)
E1	REFCLK1+	PCIe Reference Clock + (dual port, port B)		E14	PERp0	PCIe Receive+ (lane 0)
E2	REFCLK1-	PCIe Reference Clock - (dual port, port B)		E15	GND	Ground
E3	3.3V AUX	Auxiliary Power (for SMBus access)		E16	Not Used	
E4	ePERST1#	PCIe Reset (dual port, port B)		S8	Not Used	Ground
E5	ePERST0#	PCIe Reset (primary port A)		S9	Not Used	
E6	Not Used			S10	Not Used	
P1	Not Used			S11	Not Used	Ground
P2	Not Used			S12	Not Used	
P3	Not Used			S13	Not Used	
P4	IfDet #	Interface Detect		S14	Not Used	Ground
P5	GND	Ground		S15	Not Used	
P6	GND	Ground		S16	GND	Ground
P7	Not Used			S17	PETp1	PCIe Transmit+ (lane 1)
P8	Not Used			S18	PETn1	PCIe Transmit- (lane 1)
P9	Not Used			S19	GND	Ground
P10	PRSNT #	Presence		S20	PERn1	PCIe Receive- (lane 1)
P11	Activity	Drive Active		S21	PERp1	PCIe Receive+ (lane 1)
P12	GND	Ground		S22	GND	Ground
P13	12 V	Primary Power		S23	PETp2	PCIe Transmit+ (lane 2)
P14	12 V	Primary Power		S24	PETn2	PCIe Transmit- (lane 2)
P15	12 V	Primary Power		S25	GND	Ground
				S26	PERn2	PCIe Receive- (lane 2)
				S27	PERp2	PCIe Receive+ (lane 2)
				S28	GND	Ground
				E17	PETp3	PCIe Transmit+ (lane 3)
				E18	PETn3	PCIe Transmit- (lane 3)
				E19	GND	Ground
				E20	PERn3	PCIe Receive- (lane 3)
				E21	PERp3	PCIe Receive+ (lane 3)
				E22	GND	Ground
				E23	SMClk	SMBus Clock
				E24	SMDat	SMBus Data
				E25	DualPortEn#	Dual Port PCIe enable

5.0 PCI AND NVM EXPRESS REGISTERS

5.1 PCI Express Registers

5.1.1 PCI Register Summary

[Table 21] PCI Register Summary

Start Address	Tag	Name	Type
00h	TYPE0_HDR	PCI Header	PCI Configuration Header Space
40h	PM_CAP	PCI Power Management Capability	PCI Capability
50h	MSI_CAP	MSI Capability	PCI Capability
70h	PCIE_CAP	PCI Express Capability	PCI Capability
B0h	MSIX_CAP	MSI-X Capability	PCI Capability
100h	AER_CAP	Advanced Error Reporting (AER) Capability	PCIe Extended Capability
178h	SPCIE_CAP	Secondary PCI Express Capability (Gen3) Capability	PCIe Extended Capability

5.1.2 PCI Header Registers

5.1.2.1 PCI Configuration Header Space Registers

[Table 22] PCI Header Space Summary

Start Address	End Address	Symbol	Description
00h	03h	ID	Identifiers
04h	05h	CMD	Command Register
06h	07h	STS	Status Register
08h	08h	REVID	Revision ID
09h	0Bh	CC	Class Codes
0Ch	0Ch	CLS	Cache Line Size
0Dh	0Dh	MLT	Master Latency Timer
0Eh	0Eh	HTYPE	Header Type
0Fh	0Fh	BIST	Built in Self Test
10h	13h	MLBAR (BAR0)	Memory Register Base Address (lower 32-bit)
14h	17h	MUBAR (BAR1)	Memory Register Base Address (upper 32-bit)
18h	1Bh	IDBAR (BAR2)	Reserved
1Ch	1Fh	BAR3	Reserved
20h	23h	BAR4	Reserved
24h	27h	BAR5	Reserved
28h	2Bh	CCPTR	CardBus CIS Pointer
2Ch	2Fh	SS	Subsystem Identifiers
30h	33h	EXPROM	Expansion ROM Base Address
34h	34h	CAP	Capabilities Pointer
35h	3Bh	R	Reserved
3Ch	3Dh	INTR	Interrupt Information
3Eh	3Eh	MGNT	Minimum Grant
3Fh	3Fh	MLAT	Maximum Latency

[Table 23] Identifier Register

Bits	Type	Default Value	Description
31:16	RO	A822h	Device ID
0:15	RO	144Dh	Vendor ID

[Table 24] Command Register

Bits	Type	Default Value	Description
15:11	RO	0	Reserved
10	RW	0	Interrupt Disable
9	RO	0	Fast Back-to-Back Enable (N/A)
8	RW	0	SERR# Enable
7	RO	0	IDSEL Stepping / Wait Cycle Control (N/A)
6	RW	0	Parity Error Response Enable
5	RO	0	VGA Palette Snooping Enable (N/A)
4	RO	0	Memory Write and Invalidate Enable (N/A)
3	RO	0	Special Cycle Enable (N/A)
2	RW	0	Bus Master Enable
1	RW	0	Memory Space Enable
0	RW	0	I/O Space Enable

[Table 25] Status Register

Bits	Type	Default Value	Description
15	RW1C	0	Detected Parity Error
14	RW1C	0	Signaled System Error
13	RW1C	0	Received Master Abort
12	RW1C	0	Received Target Abort
11	RW1C	0	Signaled Target Abort (N/A)
10:9	RO	0	DEVSEL Timing (N/A)
8	RW1C	0	Master Data Parity Error Detected
7	RO	0	Fast Back-To-Back Capable (N/A)
6	RO	0	Reserved
5	RO	0	66MHz Capable (N/A)
4	RO	1	Capabilities List
3	RO	0	Interrupt Status
2:1	RO	0	Reserved
0	RO	0	Reserved

[Table 26] Revision ID Register

Bits	Type	Default Value	Description
7:0	RO	00h	Controller Hardware Revision ID

[Table 27] Class Code Register

Bits	Type	Default Value	Description
23:16	RO	01h	Base Class Code
15:8	RO	08h	Sub Class Code
7:0	RO	02h	Programming Interface

[Table 28] Cache Line Size Register

Bits	Type	Default Value	Description
7:0	RW	0	Cache Line Size (N/A)

[Table 29] Master Latency Timer Register

Bits	Type	Default Value	Description
7:0	RO	0	Master Latency Timer (N/A)

[Table 30] Header Type Register

Bits	Type	Default Value	Description
7	RO	0	Multi-Function Device (N/A)
6:0	RO	0	Reserved

[Table 31] Built In Self Test Register

Bits	Type	Default Value	Description
7	RO	0	Built In Self Test (N/A)
6	RO	0	Built In Self Test (N/A)
5:4	RO	0	Built In Self Test (N/A)
3:0	RO	0	Built In Self Test (N/A)

[Table 32] Memory Register Base Address Lower 32-bits (BAR0) Register

Bits	Type	Default Value	Description
31:15	RW	0	Base Address
14:4	RO	0	Reserved
3	RO	0	Pre-Fetchable
2:1	RO	2h	Address Type (64-bit)
0	RO	0	Memory Space Indicator (MEMSI)

[Table 33] Memory Register Base Address Upper 32-bits (BAR1)

Bits	Type	Default Value	Description
31:0	RW	0	Base Address

[Table 34] Memory Register Base Address (BAR2) Register

Bits	Type	Default Value	Description
31:0	RO	0	N/A

[Table 35] BAR3 Register

Bits	Type	Default Value	Description
31:0	RO	0	N/A

[Table 36] Vendor Specific BAR4 Register

Bits	Type	Default Value	Description
31:0	RO	0	N/A

[Table 37] Vendor Specific BAR5 Register

Bits	Type	Default Value	Description
31:0	RO	0	N/A

[Table 38] Cardbus CIS Pointer Register

Bits	Type	Default Value	Description
31:0	RO	0	N/A

[Table 39] Subsystem Identifier Register

Bits	Type	Default Value	Description
31:16	RO	A801h	Subsystem ID
15:0	RO	144Dh	Subsystem Vendor ID

[Table 40] Expansion ROM Register

Bits	Type	Default Value	Description
31:17	RW	0	Expansion ROM Base Address
16:1	RO	0	Reserved
0	RW	0	Expansion ROM Enable/Disable

[Table 41] Capabilities Pointer Register

Bits	Type	Default Value	Description
7:0	RO	40h	Capability Pointer

[Table 42] Interrupt Information Register

Bits	Type	Default Value	Description
15:8	RO	01h	Interrupt Pin
7:0	RW	FFh	Interrupt Line

[Table 43] Minimum Grant Register

Bits	Type	Default Value	Description
7:0	RO	0	Minimum Grant (N/A)

[Table 44] Maximum Latency Register

Bits	Type	Default Value	Description
7:0	RO	0	Maximum Latency (N/A)

5.1.3 PCI Capability Registers Detail

5.1.3.1 PCI Power Management Capability

[Table 45] PCI Power Management Capability Summary

Start Address	End Address	Symbol	Description
40h	40h	PCIPM_ID	PCI Power Management Capability ID
41h	41h	NEXTCAP	Next Capability Pointer
42h	43h	PCIPM_CAP	PC Power Management Capabilities
44h	45h	PCIPM_CS	PCI Power Management Control and Status
46h	46h	PCIPM_CSR_BSE	PMCSR_BSE Bridge Extensions
47h	47h	PCIPM_DATA	Data

[Table 46] PCI Power Management Capability ID Register

Bits	Type	Default Value	Description
15:8	RO	50h	Next Capability Pointer
7:0	RO	1h	Capability ID

[Table 47] PCI Power Management Capability Register

Bits	Type	Default Value	Description
15:11	RO	0	PME Support (N/A)
10	RO	0	D2 Support (N/A)
9	RO	0	D1 Support (N/A)
8:6	RO	0	AUX current (N/A)
5	RO	0	Device Specific Initialization (N/A)
4	RsvdP	0	Reserved
3	RO	0	PME Clock (N/A)
2:0	RO	3h	Version (Support for PCIe Power Management Interface Spec Rev. 1.2)

[Table 48] PCI Power Management Control and Status Register

Bits	Type	Default Value	Description
31:24	RsvdP	0	Data register (N/A)
23	RO	0	Bus Power / Clock Enable (N/A)
22	RO	0	B2, B3 Support (N/A)
21:16	RsvdP	0	Reserved
15	RO	0	PME Status (N/A)
14:13	RO	0	Data Scale (N/A)
12:9	RO	0	Data Scale (N/A)
8	RWS	0	PME Enable (N/A)
7:4	RsvdP	0	Reserved
3	RO	1	No Soft Reset
2	RsvdP	0	Reserved
1:0	RW	0	Power State

5.1.3.2 Message Signaled Interrupt (MSI) Registers

[Table 49] Message Signaled Interrupt Capability Summary

Start Address	End Address	Symbol	Description
50h	51h	MSI_ID	Message Signaled Interrupt Capability ID
52h	53h	MSI_MC	Message Signaled Interrupt Message Control
54h	57h	MSI_MA	Message Signaled Interrupt Message Address
58h	5Bh	MSI_MUA	Message Signaled Interrupt Upper Address
5Ch	5Dh	MSI_MDATA	Message Signaled Interrupt Message Data
60h	63h	MSI_MMASK	Message Signaled Interrupt Mask Bits
64h	67h	MSI_MPEND	Message Signaled Interrupt Pending Bits

[Table 50] Message Signaled Interrupt Capability ID Register

Bits	Type	Default Value	Description
15:8	RO	70h	Next Capability Pointer
7:0	RO	05h	Capability ID

[Table 51] Message Signaled Interrupt Control Register

Bits	Type	Default Value	Description
15:9	RsvdP	0	Reserved
8	RO	0	Per Vector Masking Capable (N/A)
7	RO	1h	64-bit Address Capable
6:4	RW	0	Multiple Message Enable
3:1	RO	5h	Multiple Message Capable
0	RW	0	MSI Enable

[Table 52] Message Signaled Interrupt Address Register

Bits	Type	Default Value	Description
31:2	RW	0	Address
1:0	RsvdP	0	Reserved

[Table 53] Message Signaled Interrupt Upper Address Register

Bits	Type	Default Value	Description
31:0	RW	0	Upper Address

[Table 54] Message Signaled Interrupt Message Data Register

Bits	Type	Default Value	Description
31:16	RsvdP	0	Reserved
15:0	RW	0	Data

[Table 55] Message Signaled Interrupt Mask Bits Register

Bits	Type	Default Value	Description
31:0	RW	0	Mask Bits (N/A)

[Table 56] Message Signaled Interrupt Pending Bits Register

Bits	Type	Default Value	Description
31:0	RO	0	Pending Bits

5.1.3.3 MSI-X Capability

[Table 57] MSI-X Capability Register Summary

Start Address	End Address	Symbol	Description
B0h	B1h	MSIX_ID	MSI-X Capability ID
B2h	B3h	MSIX_CAP	MSI-X Message Control
B4h	B7h	MSIX_TBL	MSI-X Table Offset and Table BIR
B8h	BBh	MSIX_PBA	MSI-X PBA Offset and PBA BIR

[Table 58] MSI-X Capability ID Register

Bits	Type	Default Value	Description
15:8	RO	00h	Next Capability Pointer
7:0	RO	11h	Capability ID

[Table 59] MSI-X Control Register

Bits	Type	Default Value	Description
15	RW	0	MSI-X Enable
14	RW	0	Function Mask
13:11	RsvdP	0	Reserved
10:0	RO	243h	Table Size

[Table 60] MSI-X Table Offset Register

Bits	Type	Default Value	Description
31:3	RO	800h	Table Offset
2:0	RO	0	Table BIR

[Table 61] MSI-X Pending Bit Array Offset Register

Bits	Type	Default Value	Description
31:3	RO	600h	Pending Bit Array Offset
2:0	RO	0	Pending Bit Array BIR

5.1.3.4 PCI Express Capability Registers

[Table 62] PCI Express Capability Register Summary

Start Address	End Address	Symbol	Description
70h	71h	PCIe _ID	PCI Express Capability ID
72h	73h	PCIe_CAP	PCI Express Capabilities
74h	77h	PCIe_DCAP	PCI Express Device Capabilities
78h	79h	PCIe_DC	PCI Express Device Control
7Ah	7Bh	PCIe_DS	PCI Express Device Status
7Ch	7Fh	PCIe_LCAP	PCI Express Link Capabilities
80h	81h	PCIe_LC	PCI Express Link Control
82h	83h	PCIe_LS	PCI Express Link Status
94h	97h	PCIe_DCAP2	PCI Express Device Capabilities 2
98h	99h	PCIe_DC2	PCI Express Device Control 2
9Ah	9Bh	PCIe_DS2	PCI Express Device Status 2
9Ch	9Fh	PCIe_LCAP2	PCI Express Link Capabilities 2
A0h	A1h	PCIe_LC2	PCI Express Link Control 2
A2h	A3h	PCIe_LS2	PCI Express Link Status 2

[Table 63] PCI Express Capability ID Register

Bits	Type	Default Value	Description
15:8	RO	B0h	Next Capability Pointer
7:0	RO	10h	Capability ID

[Table 64] PCI Express Capabilities Register

Bits	Type	Default Value	Description
15:14	RsvdP	0	Reserved
13:9	RO	0	Interrupt Message Number
8	HwInit	0	Slot Implementation (N/A)
7:4	RO	0	Device/Port Type
3:0	RO	2h	Capability Version

[Table 65] PCI Express Device Capabilities Register

Bits	Type	Default Value	Description
31:29	RsvdP	0	Reserved
28	RO	1	Function Level Reset Capability
27:26	RO	0	Captured Slot Power Limit Scale
25:18	RO	0	Captured Slot Power Limit Value
17:16	RsvdP	0	Reserved
15	RO	1	Role-based Error Reporting
14:12	RO	0	Reserved
11:9	RO	7h	Endpoint L1 Acceptable Latency
8:6	RO	7h	Endpoint L0 Acceptable Latency
5	RO	0	Extended Tag Field Supported
4:3	RO	0	Phantom Functions Supported
2:0	RO	2h	Max Payload Size Supported

[Table 66] PCI Express Device Control Register

Bits	Type	Default Value	Description
15	RW	0	Initiate Function Level Reset
14:12	RW	2h	Max Read Request Size
11	RW	1	Enable No Snoop
10	RWS	0	Aux Power PM Enable (N/A)
9	RW	0	Phantom Functions Enable (N/A)
8	RW	0	Extended Tag Enable
7:5	RW	0	Max Payload Size
4	RW	1	Enable Relaxed Ordering
3	RW	0	Unsupported Request Reporting Enable
2	RW	0	Fatal Error Reporting Enable
1	RW	0	Non-Fatal Error Reporting Enable
0	RW	0	Correctable Error Reporting Enable

[Table 67] PCI Express Device Status Register

Bits	Type	Default Value	Description
15:6	RsvdZ	0	Reserved
5	RO	0	Transactions Pending
4	RO	0	Aux Power Detected
3	RW1C	0	Unsupported Request Detected
2	RW1C	0	Fatal Error Detected
1	RW1C	0	Non-Fatal Error Detected
0	RW1C	0	Correctable Error Detected

[Table 68] PCI Express Link Capabilities Register

Bits	Type	Default Value	Description
31:24	HwInit	0 (Port 0)	Port Number
23	RsvdP	0	Reserved
22	HwInit	1	ASPM Optionality Compliance
21	RO	0	Link Bandwidth Notification Capability (N/A)
20	RO	0	Data Link Layer Link Active Reporting Capable (N/A)
19	RO	0	Surprise Down Error Reporting Capable (N/A)

18	RO	0	Clock Power Management
17:15	RO	6h	L1 Exit Latency
14:12	RO	7h	L0s Exit Latency
11:10	RO	0	Active State Power Management Support
9:4	RO	4h (x4 link)	Maximum Link Width
3:0	RO	3h	Supported Link Speeds

[Table 69] PCI Express Link Control Register

Bits	Type	Default Value	Description
15:14	RW/RsvdP	0h	Reserved
13:12	RsvdP	0	Reserved
11	RsvdP	0	Link Autonomous Bandwidth interrupt enable (N/A)
10	RsvdP	0	Link Bandwidth management interrupt enable (N/A)
9	RW	0	Hardware Autonomous Width Disable
8	RW	0	Enable Clock Power Management
7	RW	0	Extended Sync
6	RW	0	Common Clock Configuration
5	RsvdP	0	Retrain Link (N/A)
4	RsvdP	0	Link Disable (N/A)
3	RW	0	Read Completion Boundary (N/A)
2	RsvdP	0	Reserved
1:0	RW	0	Active State Power Management Control

[Table 70] PCI Express Link Status Register

Bits	Type	Default Value	Description
15	RsvdP	0h	Link Autonomous Bandwidth Status (N/A)
14	RsvdP	0	Link Autonomous Management Status (N/A)
13	RO	0	Data Link Layer Link Active
12	HwInit	1	Slot Clock Configuration
11	RO	0	Link Training (N/A)
10	RO	0	Reserved
9:4	RO	1h	Negotiated Link Width
3:0	RO	1h	Current Link Speed

[Table 71] PCI Express Device Capabilities 2 Register

Bits	Type	Default Value	Description
31	HwInit	0	Reserved
30:24	RsvdP	0	Reserved
23:22	HwInit	0	Max End-End TLP Prefixes (N/A)
21	HwInit	0	End-End TLP Prefix Supported (N/A)
20	RO	0	Extended Format Field Supported (N/A)
19:18	HwInit	0	OBFF Supported (N/A)
17:16	RsvdP	0	Reserved
15:14	HwInit	0	LN System CLS (N/A)
13:12	RO	0	TPH Completer Supported (N/A)
11	RO	0	Latency Tolerance Reporting Supported
10	HwInit	0	No RO-enabled PR-PR Passing (N/A)
9	RO	0	128-bit CAS Completer Supported (N/A)

8	RO	0	64-bit Atomic Op Completer Supported (N/A)
7	RO	0	32-bit Atomic Op Completer Supported (N/A)
6	RO	0	Atomic Op Routing Supported (N/A)
5	RO	0	ARI Forwarding Supported (N/A)
4	RO	1	Completion Timeout Disable Supported
3:0	HwInit	Fh	Completion Timeout Ranges Supported

[Table 72] PCI Express Device Control 2 Register

Bits	Type	Default Value	Description
15	RsvdP	0	End-to-end Prefix Blocking (N/A)
14:13	RW/RsvdP	0	OBFF Enable (N/A)
12:11	RsvdP	0	Reserved
10	RW/RsvdP	0	Latency Tolerance Reporting Mechanism Enable
9	RW	0	IDO Completion enable (N/A)
8	RW	0	IDO Request Enable (N/A)
7	RW	0	AtomicOp Egress Blocking (N/A)
6	RW	0	AtomicOp Requester Enable (N/A)
5	RW	0	ARI forwarding supported (N/A)
4	RW	0	Completion Timeout Disable
3:0	RW	0	Completion Timeout Value

[Table 73] PCI Express Device Status 2 Register

Bits	Type	Default Value	Description
15:0	RsvdZ	0	Reserved

[Table 74] PCI Express Link Capabilities 2 Register

Bits	Type	Default Value	Description
31	RO	0	Reserved
30:24	RsvdP	0	Reserved
23	HwInit	0	Reserved
22:16	HwInit	0	Lower SKP OS Reception Supported Speed Vector (N/A)
15:9	HwInit	0	Lower SKP OS Generation Supported Speed Vector (N/A)
8	RO	0	Cross-Link Supported (N/A)
7:1	RO	7h	Supported Speeds Vector
0	RsvdP	0	Reserved

[Table 75] PCI Express Link Control 2 Register

Bits	Type	Default Value	Description
15:12	RWS/RsvdP	0	Compliance De-emphasis
11	RWS/RsvdP	0	Compliance SOS
10	RWS/RsvdP	0	Enter Modified Compliance
9:7	RWS/RsvdP	0	Transmit Margin
6	HwInit	0	Select De-Emphasis (N/A)
5	RWS/RsvdP	0	Hardware Autonomous Speed Disable
4	RWS/RsvdP	0	Enter Compliance
3:0	RWS/RsvdP	3h	Target Link Speed

[Table 76] PCI Express Link Status 2 Register

Bits	Type	Default Value	Description
15:6	RsvdP	0	Reserved
5	RW1CS	0	Link Equalization Request
4	ROS	0	Equalization 8.0GT/s Phase 3 Successful
3	ROS	0	Equalization 8.0GT/s Phase 2 Successful
2	ROS	0	Equalization 8.0GT/s Phase 1 Successful
1	ROS	0	Equalization Complete
0	RO	1	Current De-Emphasis

5.1.4 PCI Extended Capability Details

5.1.4.1 Advanced Error Reporting Registers

[Table 77] Advanced Error Reporting Capability Summary

Start Address	End Address	Symbol	Description
100h	103h	AER_ID	AER Capability ID
104h	107h	AER_UCES	AER Uncorrectable Error Status
108h	10Bh	AER_UCEM	AER Uncorrectable Error Mask
10Ch	10Fh	AER_UCESEV	AER Uncorrectable Error Severity
110h	113h	AER_CES	AER Correctable Error Status
114h	117h	AER_CEM	AER Correctable Error Mask
118h	11Bh	AER_CC	AER Advanced Error Capabilities and Control
11Ch	12Bh	AER_HL	AER Header Log

[Table 78] AER Capability ID Register

Bits	Type	Default Value	Description
31:20	RO	178h	Next Capability Pointer
19:16	RO	2h	Capability Version
15:0	RO	1h	PCI Express Extended Capability ID

[Table 79] AER Uncorrectable Error Status Register

Bits	Type	Default Value	Description
31:27	RsvdZ	0	Reserved
26	RW1CS	0	Poisoned TLP Egress Blocked Status (N/A)
25	RW1CS	0	TLP Prefix Blocked Error Status (N/A)
24	RW1CS	0	Atomic Op Egress Blocked Status (N/A)
23	RW1CS	0	MC Blocked TLP Status (N/A)
22	RW1CS	0	Uncorrectable Internal Error Status
21	RW1CS	0	ACS Violation Status (N/A)
20	RW1CS	0	Unsupported Request Error Status
19	RW1CS	0	ECRC Error Status
18	RW1CS	0	Malformed TLP Status
17	RW1CS	0	Receiver Overflow Status
16	RW1CS	0	Unexpected Completion Status
15	RW1CS	0	Completer Abort Status
14	RW1CS	0	Completion Timeout Status
13	RW1CS	0	Flow Control Protocol Error Status
12	RW1CS	0	Poisoned TLP Status

11:6	RsvdZ	0	Reserved
5	RW1CS	0	Surprise Down Error Status (N/A)
4	RW1CS	0	Data Link Protocol Error Status
3:1	RsvdZ	0	Reserved
0	Undefined	0	Undefined

[Table 80] AER Uncorrectable Error Mask Register

Bits	Type	Default Value	Description
31:27	RsvdZ	0	Reserved
26	RWS	0	Poisoned TLP Egress Blocked Mask (N/A)
25	RWS	0	TLP Prefix Blocked Error Mask (N/A)
24	RWS	0	Atomic Op Egress Blocked Mask (N/A)
23	RWS	0	Uncorrectable Internal Error Mask
22	RWS	1	Uncorrectable Internal Error Mask
21	RWS	0	ACS Violation Mask (N/A)
20	RWS	0	Unsupported Request Error Mask
19	RWS	0	ECRC Error Mask
18	RWS	0	Malformed TLP Mask
17	RWS	0	Receiver Overflow Mask
16	RWS	0	Unexpected Completion Mask
15	RWS	0	Completer Abort Mask
14	RWS	0	Completion Timeout Mask
13	RWS	0	Flow Control Protocol Error Mask
12	RWS	0	Poisoned TLP Mask
11:6	RsvdZ	0	Reserved
5	RWS	0	Surprise Down Error Mask (N/A)
4	RWS	0	Data Link Protocol Error Mask
3:1	RsvdZ	0	Reserved
0	Undefined	0	Undefined

[Table 81] AER Uncorrectable Error Severity Register

Bits	Type	Default Value	Description
31:27	RsvdP	0	Reserved
26	RWS	0	Poisoned TLP Egress Blocked Severity (N/A)
25	RWS	0	TLP Prefix Blocked Error Severity (N/A)
24	RWS	0	Atomic Op Egress Blocked Severity (N/A)
23	RWS	0	MC Blocked TLP Severity (N/A)
22	RWS	1	Uncorrectable Internal Error Severity
21	RWS	0	ACS Violation Severity (N/A)
20	RWS	0	Unsupported Request Error Severity
19	RWS	0	ECRC Error Severity
18	RWS	1	Malformed TLP Severity
17	RWS	1	Receiver Overflow Severity
16	RWS	0	Unexpected Completion Severity
15	RWS	0	Completer Abort Severity
14	RWS	0	Completion Timeout Severity
13	RWS	1	Flow Control Protocol Error Severity

12	RWS	0	Poisoned TLP Severity
11:6	RsvdP	0	Reserved
5	RWS	1	Surprise Down Error Severity (N/A)
4	RWS	1	Data Link Protocol Error Severity
3:1	RsvdP	0	Reserved
0	Undefined	0	Undefined

[Table 82] AER Correctable Error Status Register

Bits	Type	Default Value	Description
31:16	RsvdZ	0	Reserved
15	RW1CS	0	Header Log Overflow Status
14	RW1CS	0	Corrected Internal Error Status
13	RW1CS	0	Advisory Non-Fatal Error Status
12	RW1CS	0	Replay Timer Timeout Status
11:9	RsvdZ	0	Reserved
8	RW1CS	0	Replay Number Rollover Status
7	RW1CS	0	Bad DLLP Status
6	RW1CS	0	Bad TLP Status
5:1	RsvdZ	0	Reserved
0	RW1CS	0	Received Error Status

[Table 83] AER Correctable Error Mask Register

Bits	Type	Default Value	Description
31:16	RsvdP	0	Reserved
15	RWS	1	Header Log Overflow Mask
14	RWS	1	Corrected Internal Error Mask
13	RWS	1	Advisory Non-Fatal Error Mask
12	RWS	0	Replay Timer Timeout Mask
11:9	RsvdP	0	Reserved
8	RWS	0	Replay Number Rollover Mask
7	RWS	0	Bad DLLP Mask
6	RWS	0	Bad TLP Mask
5:1	RsvdP	0	Reserved
0	RWS	0	Received Error Mask

[Table 84] AER Capabilities and Control Register

Bits	Type	Default Value	Description
31:13	RsvdP	0	Reserved
12	RO	0	Completion Timeout Prefix / Header Log Capable (N/A)
11	ROS	0	TLP Prefix Log Present (N/A)
10	RWS	0	Multiple Header Recording Enable
9	RO	1	Multiple Header Recording Capable
8	RWS	0	ECRC Check Enable
7	RO	1	ECRC Check Capable
6	RWS	0	ECRC Generation Enable
5	RO	1	ECRC Generation Capable
4:0	ROS	0	First Error Pointer

[Table 85] AER Header Log Register

Bits	Type	Default Value	Description
127:120	ROS	0	Header Byte 0
119:112	ROS	0	Header Byte 1
111:104	ROS	0	Header Byte 2
103:96	ROS	0	Header Byte 3
95:88	ROS	0	Header Byte 4
87:80	ROS	0	Header Byte 5
79:72	ROS	0	Header Byte 6
71:64	ROS	0	Header Byte 7
63:56	ROS	0	Header Byte 8
55:48	ROS	0	Header Byte 9
47:40	ROS	0	Header Byte 10
39:32	ROS	0	Header Byte 11
31:24	ROS	0	Header Byte 12
23:16	ROS	0	Header Byte 13
15:8	ROS	0	Header Byte 14
7:0	ROS	0	Header Byte 15

5.1.4.2 Secondary PCI Express Capability

[Table 86] Secondary PCI Express Capability Summary

Start Address	End Address	Symbol	Description
178h	17Bh	SPE_ID	Secondary PCI Express Capability Header
17Ch	17Fh	SPE_LC#	PCI Express Link Control 3
180h	183h	SPE_LE	PCI Express Lane Error Status
184h	185h	SPE_L0EC	PCI Express Lane 0 Equalization Control
186h	187h	SPE_L1EC	PCI Express Lane 1 Equalization Control
188h	189h	SPE_L2EC	PCI Express Lane 2 Equalization Control
18Ah	18Bh	SPE_L3EC	PCI Express Lane 3 Equalization Control

[Table 87] Secondary PCI Express Capability ID Register

Bits	Type	Default Value	Description
31:20	RO	000h	Next Capability Offset
19:16	RO	1h	Capability Version
15:0	RO	19h	Capability ID (Secondary PCI Express Extended capability)

[Table 88] PCI Express Link Control 3 Register

Bits	Type	Default Value	Description
31:16	RsvdP	0	Reserved
15:9	RW	0	Enable Lower SKP OS Generation Vector (N/A)
8:2	RsvdP	0	RsvdP
1	RW	0	Link Equalization Request Interrupt Enable (N/A)
0	RW	0	Perform Equalization (N/A)

[Table 89] PCI Express Lane Error Status Register

Bits	Type	Default Value	Description
31:4	RsvdP	0	Reserved
3:0	RW1CS	0	Lane Error Status Bits

[Table 90] PCI Express Lane 0 Equalization Register

Bits	Type	Default Value	Description
15	RsvdP	0	Reserved
14:12	HwInit/RO	7h	Upstream Port 8.0T/s Receiver Preset Hint
11:8	HwInit/RO	Fh	Upstream Port 8.0T/s Transmitter Preset
7	RsvdZ	0	Reserved
6:4	HwInit/RsvdP	0	Downstream Port 8.0T/s Receiver Preset Hint (N/A)
3:0	HwInit/RsvdP	0	Downstream Port 8.0T/s Transmitter Preset (N/A)

[Table 91] PCI Express Lane 1 Equalization Register

Bits	Type	Default Value	Description
15	RsvdP	0	Reserved
14:12	HwInit/RO	7h	Upstream Port 8.0T/s Receiver Preset Hint
11:8	HwInit/RO	Fh	Upstream Port 8.0T/s Transmitter Preset
7	RsvdZ	0	Reserved
6:4	HwInit/RsvdP	0	Downstream Port 8.0T/s Receiver Preset Hint (N/A)
3:0	HwInit/RsvdP	0	Downstream Port 8.0T/s Transmitter Preset (N/A)

[Table 92] PCI Express Lane 2 Equalization Register

Bits	Type	Default Value	Description
15	RsvdP	0	Reserved
14:12	HwInit/RO	7h	Upstream Port 8.0T/s Receiver Preset Hint
11:8	HwInit/RO	Fh	Upstream Port 8.0T/s Transmitter Preset
7	RsvdZ	0	Reserved
6:4	HwInit/RsvdP	0	Downstream Port 8.0T/s Receiver Preset Hint (N/A)
3:0	HwInit/RsvdP	0	Downstream Port 8.0T/s Transmitter Preset (N/A)

[Table 93] PCI Express Lane 3 Equalization Register

Bits	Type	Default Value	Description
15	RsvdP	0	Reserved
14:12	HwInit/RO	7h	Upstream Port 8.0T/s Receiver Preset Hint
11:8	HwInit/RO	Fh	Upstream Port 8.0T/s Transmitter Preset
7	RsvdZ	0	Reserved
6:4	HwInit/RsvdP	0	Downstream Port 8.0T/s Receiver Preset Hint (N/A)
3:0	HwInit/RsvdP	0	Downstream Port 8.0T/s Transmitter Preset (N/A)

5.2 NVM Express Registers

5.2.1 Register Summary

[Table 94] Register Summary

Start Address	End Address	Name	Type
00h	07h	CAP	Controller Capabilities
08h	0Bh	VS	Version
0Ch	0Fh	INTMS	Interrupt Mask Set
10h	13h	INTMC	Interrupt Mask Clear
14h	17h	CC	Controller Configuration
18h	1Bh	Reserved	Reserved
1Ch	1Fh	CSTS	Controller Status
20h	23h	Reserved	Reserved
24h	27h	AQA	Admin Queue Attributes
28h	2Fh	ASQ	Admin Submission Queue Base Address
30h	37h	ACQ	Admin Completion Queue Base Address
38h	EFFh	Reserved	Reserved
F00h	FFFh	Reserved	Command Set Specific
1000h	1003h	SQ0TDBL	Submission Queue 0 Tail Doorbell (Admin)
1000h + (1 * (4 << CAP.DSTRD))	1003h + (1 * (4 << CAP.DSTRD))	CQ0HDBL	Completion Queue 0 Head Doorbell (Admin)
...			
1000h+ (2y * (4 << CAP.DSTRD))	1003h + (2y * (4 << CAP.DSTRD))	SQyTDBL	Submission Queue y Tail Doorbell
1000h + ((2y + 1) * (4 << CAP.DSTRD))	1003h + ((2y + 1) * (4 << CAP.DSTRD))	CQYHDBL	Completion Queue y Head Doorbell

5.2.2 Controller Registers

[Table 95] Controller Capabilities

Bits	Type	Name	Default Value	Description
63:56	RO	-	0h	Reserved
55:52	RO	MPSMAX	0Fh	Memory Page Size Maximum ((2 ^ (12 + MPSMAX)).
51:48	RO	MPSMIN	0	Memory Page Size Minimum (2 ^ (12 + MPSMIN)).
47:41	RO	-	0	Reserved
40:37	RO	CSS	1h	Command Sets Supported 1h: NVM command set
36	RO	NSSRS	1	NVM Subsystem Reset Supported (NSSRS)
35:32	RO	DSTRD	0	Doorbell Stride 0: Stride of 4 bytes
31:24	RO	TO	78h	Timeout (This field is in 500 millisecond units)
23:19	RO	-	0	Reserved
18:17	RO	AMS	1	Arbitration Mechanism Supported
16	RO	CQR	1	Contiguous Queues Required
15:0	RO	MQES	3FFh	Maximum Queue Entries Supported

[Table 96] Version

Bits	Type	Name	Default Value	Description
31:16	RO	MJR	1h	Major Version Number
15:0	RO	MNR	200h	Minor Version Number

NOTE:
The SZ1735 supports NVM Express version 1.1c.

[Table 97] Interrupt Mask Set

Bits	Type	Name	Default Value	Description
31:00	RW1S	IVMS	1h	Interrupt Vector Mask Set

[Table 98] Interrupt Mask Clear

Bits	Type	Name	Default Value	Description
31:00	RW1C	IVMC	1h	Interrupt Vector Mask Clear

[Table 99] Controller Configuration

Bits	Type	Name	Default Value	Description
31:24	RO	-	0	Reserved
23:20	RW	IOCQES	4	I/O Completion Queue Entry Size (Configured as a power of 2) (Should be set to 4 for a 16 byte entry size)
19:16	RW	IOSQES	6	I/O Submission Queue Entry Size (Configured as a power of 2) (Should be set to 6 for a 64 byte entry size)
15:14	RW	SHN	0	Shutdown Notification 0h: No notification 1h: Normal shutdown notification 2h: Abrupt shutdown notification 3h: Reserved CSTS.SHST indicates shutdown status.
13:11	RW	AMS	0	Arbitration Mechanism Selected 0h: Round Robin No other values supported.
10:7	RW	MPS	0	Memory Page Size MPS is 2^(12+MPS) Shall be within CAP.MPSMAX and CAP.MPSMIN ranges.
6:4	RW	CSS	0	Command Set Selected 0h: NVM Command Set No other values supported
3:1	RO	-	0	Reserved
0	RW	EN	0	Enable When set to 1, controller shall process commands. When cleared to 0, controller shall not process commands. This field is subject to CSTS.RDY and CAP.TO restrictions.

[Table 100] Controller Status

Bits	Type	Name	Default Value	Description
31:6	RO	-	0	Reserved
5	RO	PP	0	Processing Paused
4	RW1C	NSSRO	0	NVM Subsystem Reset Occurred
3:2	RO	SHST	0	Shutdown Status 0h: Normal operation, no shutdown requested 1h: Shutdown processing occurring 2h: Shutdown processing complete 3h: Reserved
1	RO	CFS	0	Controller Fatal Status
0	RO	RDY	0	1h: Controller ready to process commands 0h: Controller shall not process commands.

[Table 101] Admin Queue Attributes

Bits	Type	Name	Default Value	Description
31:28	RO	-	0	Reserved
27:16	RW	ACQS	0	Admin Completion Queue Size Max: 4096 (Value of 4095h - 0's based value)
15:12	RO	-	0	Reserved
11:0	RW	ASQS	0	Admin Submission Queue Size Max: 4096 (Value of 4095h - 0's based value)

[Table 102] Admin Submission Queue Base Address

Bits	Type	Name	Default Value	Description
63:12	RW	ASQB	0	Admin Submission Queue Base Address
11:0	RO	-	0	Reserved

[Table 103] Admin Completion Queue Base Address

Bits	Type	Name	Default Value	Description
63:12	RW	ACQB	0	Admin Completion Queue Base Address
11:0	RO	-	0	Reserved

[Table 104] Submission Queue Tail y Doorbell

Bits	Type	Name	Default Value	Description
31:16	RO		0	Reserved
15:0	RW	SQT	0	Submission Queue Tail

[Table 105] Completion Queue Head y Doorbell

Bits	Type	Name	Default Value	Description
31:16	RO		0	Reserved
15:0	RW	CQH	0	Completion Queue Head

6.0 SUPPORTED COMMAND SET.

6.1 Admin Command Set

[Table 106] Opcode for Admin Commands

Opcode (Hex)	Command Name
00h	Delete I/O Submission Queue
01h	Create I/O Submission Queue
02h	Get Log Page - Error Information (01h) - SMART/Health Information (02h) - Firmware Slot Information (03h, M)
04h	Delete I/O Completion Queue
05h	Create I/O Completion Queue
06h	Identify
08h	Abort
09h	Set Feature - Arbitration (01h) - Power Management (02h) - LBA Range Type (03h) - Temperature Threshold (04h) - Error Recovery (05h) - Number of Queues (07h) - Interrupt Coalescing (08h) - Interrupt Vector Configuration (09h) - Write Atomicity (0Ah) - Asynchronous Event Configuration (0Bh) - Software Progress Marker (80h)
0Ah	Get Feature - Arbitration (01h) - LBA Range Type (03h) - Temperature Threshold (04h) - Error Recovery (05h) - Number of Queues (07h) - Interrupt Coalescing (08h) - Interrupt Vector Configuration (09h) - Write Atomicity (0Ah) - Asynchronous Event Configuration (0Bh) - Software Progress Marker (80h)
0Ch	Asynchronous Event Request
10h	Firmware Activate
11h	Firmware Image Download
80h	Format NVM
81h – BFh	I/O Command Set Specific

6.1.1 Identify Command

The Identify Command returns the data described below.

[Table 107] Identify Controller Data Structure

Bytes	O/M	Default Value	Description
1:0	M	144Dh	PCI Vendor ID
3:2	M	108Eh	PCI Subsystem Vendor ID
23:4	M	SXXXNXXXXXXXX	Serial Number (ASCII), X: Variables
63:24	M	800GB:MZWJJ800HMGQ-00007 1.6TB:MZWJJ1T6HMGG-00007 3.2TB:MZWJJ3T2HMHN-00007	Model Number (ASCII)
71:64	M	########	Firmware Revision, #: Variables
72	M	8h	Recommended Arbitration Burst
75:73	M	002538h	IEEE OUI Byte 73 - 38h Byte 74 - 25h Byte 75 - 0h
76	O	3h	Multi-Interface Capabilities 0h: Not supported (single port) 1h: Supported (dual port – future value)
77	M	5h	Maximum Data Transfer Size 0h: No restrictions
79:78	M	0h	Controller ID (CNTLID)
83:80	M	10200h	Version (VER)
87:84	M	0h	RTD3 Resume Latency (RTD3R)
91:88	M	0h	RTD3 Entry Latency (RTD3E)
95:92	M	0h	Optional Asynchronous Event Supported (OAES)
239:96		-	Reserved
255:240		Refer to the NVMe Management Interface Specification for definition.	
257:256	M	07h	Optional Admin Command Support Bits 15:3 - Reserved Bit 3: Namespace Management and Namespace Attachment command Supported Bit 2: 1h – Firmware Activate/Download Supported Bit 1: 1h Format NVM Supported Bit 0: 0 Security Send and Security Receive Not Supported (TBD)
258	M	7h	Abort Command Limit (Maximum number of concurrently outstanding Abort commands) (0's based value)
259	M	Fh	Asynchronous Event Request Limit (Maximum number of concurrently outstanding Asynchronous Event Request commands) (0's based value)
260	M	2h	Firmware Updates Bits 7:4 – Reserved Bits 3:1 – Number of firmware slots Bit 0 – 1h Slot 1 is read only
261	M	0h	Log Page Attributes Bits 7:1 – Reserved Bit 0: 0h SMART data is global for all Namespaces
262	M	FFh	Error Log Page Entries (Number of Error Information log entries stored by controller) (0's based value)
263	M	0h	Number of Power States Support (0's based value)
264	M	1h	Admin Vendor Specific Command Configuration Bits 7:1 – reserved Bit 0 – Indicates Admin Vendor Specific Commands use the format defined in NVM Express 1.1b Figure 8.

265	O	0h	Autonomous Power State Transition Attributes (APSTA)
267:266	M	160h	Warning Composite Temperature Threshold (WCTEMP)
269:268	M	167h	Critical Composite Temperature Threshold (CCTEMP)
271:270	O	78h	Maximum Time for Firmware Activation (MTFA)
275:272	O	0h	Host Memory Buffer Preferred Size (HMPRE):
279:276	O	0h	Host Memory Buffer Minimum Size (HMMIN):
295:280	O	800GB:BA4D9D6000 1.6TB:1749A956000 3.2TB:2E934856000	Total NVM Capacity (TNVMCAP):
311:296	O	0h	Unallocated NVM Capacity (UNVMCAP):
315:312	O	0h	Replay Protected Memory Block Support (RPMBS):
511:316	-	-	Reserved
512	M	66h	Submission Queue Entry Size Bits 7:4 – 6h Max SQES (64 bytes) Bits 3:0 – 6h Required SQES (64 bytes)
513	M	44h	Completion Queue Entry Size Bits 7:4 – 4h Max SQES (16 bytes) Bits 3:0 – 4h Required SQES (16 bytes)
515:514	-	-	Reserved
519:516	M	1h	Number of Namespaces
521:520	M	4h	Optional NVM Command Support Bits 51:3 – Reserved Bit 2 – 1h Dataset Management Supported Bit 1 – 0h Write Uncorrectable Supported Bit 0 – 0h Compare Not Supported
523:522	M	0h	Fused Operation Support Bits 15:1 – Reserved Bit 0 – 0h Compare/Write Fused Operation Not Supported
524	M	6h	Format NVM Attributes Bits 7:3 – Reserved Bit 2 – 1h Cryptographic Erase Bit 1 – 1h Secure Erase is applied for All Namespaces Bit 0 – 0h Format Per Namespace
525	M	0h	Volatile Write Cache 0h – No VWC present
527:526	M	FFFFh	Atomic Write Unit Normal All commands atomic
529:528	M	0h	Atomic Write Unit Power Fail (0's based value)
530	M	1h	NVM Vendor Specific Command Configuration Bits 7:1 – reserved Bit 0 – Indicates NVM Vendor Specific Commands use the format defined in NVM Express 1.2 Figure 8.
531	M	-	Reserved
533:532	O	0h	Atomic Compare & Write Unit (ACWU)
535:534	M	-	Reserved
539:536	O	0h	SGL Support (SGLS)
703:540	M	-	Reserved
I/O Command Set Attributes			
2047:704	-	-	Reserved
Power State Descriptors			
2079:2048	M	-	Power State 0 Descriptor
2111:2080	O	-	Power State 1 Descriptor (N/A)
…	-		
3071:3040	O	-	Power State 31 Descriptor (N/A)
4095:3072	-	0h	Samsung Reserved

[Table 108] Identify Power State Descriptor Data Structure

Bytes	Default Value	Description
255:125	0	Reserved
124:120	0	Relative Write Latency
119:117	0	Reserved
116:112	0	Relative Write Throughput
111:109	0	Reserved
108:104	0	Relative Read Latency
103:101	0	Reserved
100:96	0	Relative Read Throughput
95:64	100	Exit Latency (100us)
63:32	100	Entry Latency (100us)
31:16	0	Reserved
15:00	09C4h	Maximum Power (25W)

[Table 109] Identify Namespace Data Structure

Bytes	O/M	Default Value	Description
7:0	M	800GB:5D26CEB0 (512B), BA4D9D6 (4096) 1.6TB:BA4D4AB0 (512B), 1749A956 (4096) 3.2TB:1749A42B0 (512B), 2E934856 (4096)	Namespace Size
15:8	M	800GB:5D26CEB0 (512B), BA4D9D6 (4096) 1.6TB:BA4D4AB0 (512B), 1749A956 (4096) 3.2TB:1749A42B0 (512B), 2E934856 (4096)	Namespace Capacity
23:16	M	800GB:5D26CEB0 (512B), BA4D9D6 (4096) 1.6TB:BA4D4AB0 (512B), 1749A956 (4096) 3.2TB:1749A42B0 (512B), 2E934856 (4096)	Namespace Utilization
24	M	0h	Namespace Features Bits 7:1 Reserved Bit 0: Thin provisioning not supported
25	M	3h	Number of LBA Formats
26	M	10h	Formatted LBA Size Bits 7:5 – Reserved Bit 4: Metadata interleaved or separate (based on LBA format) Bit 3:0 – Indicates LBA format
27	M	3h	Metadata Capabilities Bits 7:2 – Reserved Bit 1 – Supports Metadata as separate buffer Bit 0 – Supports Metadata as extended LBA
28	M	1Fh	End-to-end Data Protection Capabilities Bits 7:5 – Reserved Bit 4 – Supports protection information as last 8 bytes of Metadata Bit 3 – Supports protection information as first 8 bytes of Metadata Bit 2 – Supports Type 3 protection information Bit 1 – Supports Type 2 protection information Bit 0 – Supports Type 1 protection information

29	M	0h	End-to-End Data Protection Type Settings Bits 7:4 – Reserved Bit 3 – 1: Protection information transferred as first 8 bytes of Metadata Bit 3 – 0: Protection information transferred as last 8 bytes of Metadata Bit 2:0 – 000b: Protection information disabled Bit 2:0 – 1h: Protection type 1 enabled Bit 2:0 – 2h: Protection type 2 enabled Bit 2:0 – 3h: Protection type 3 enabled
30		0h	Namespace Multi-path I/O and Namespace Sharing Capabilities (NMIC):
31		0h	Reservation Capabilities (RESCAP):
32		0h	Format Progress Indicator (FPI)
33		-	Reserved
35:34	O	0h	Namespace Atomic Write Unit Normal (NAWUN)
37:36	O	0h	Namespace Atomic Write Unit Power Fail (NAWUPF)
39:38	O	0h	Namespace Atomic Compare & Write Unit (NACWU)
41:40	O	0h	Namespace Atomic Boundary Size Normal (NABSN)
43:42	O	0h	Namespace Atomic Boundary Offset (NABO)
45:44	O	0h	Namespace Atomic Boundary Size Power Fail (NABSPF)
47:46	-	-	Reserved
63:48		800GB:BA4D9D6000 1.6TB:1749A956000 3.2TB:2E934856000	NVM Capacity (NVMCAP)
103:64	-	-	Reserved
119:104	O	0h	Namespace Globally Unique Identifier (NGUID)
127:120	O	TBD	IEEE Extended Unique Identifier(EUI64)
131:128	M	1090000h	LBA Format 0 Support
135:132	O	3090008h	LBA Format 1 Support
139:136	O	C0000h	LBA Format 2 Support
143:140	O	20C0008h	LBA Format 3 Support
147:144	O	-	LBA Format 4 Support (N/A)
…			
191:188	O	-	LBA Format 15 Support (N/A)
383:192	-	-	Reserved
Vendor Specific			
4095:384	-	-	Samsung Reserved

[Table 110] LBA Format 0 Data Structure

Bits	Name	Default Value	Description
31:26		0h	Reserved
25:24	RP	1h	Relative Performance
23:16	LBADS	9h	LBA Data Size
15:00	MS	0h	Metadata Size

[Table 111] LBA Format 1 Data Structure

Bits	Name	Default Value	Description
31:26		0h	Reserved
25:24	RP	3h	Relative Performance
23:16	LBADS	9h	LBA Data Size
15:00	MS	8h	Metadata Size

[Table 112] LBA Format 2 Data Structure

Bits	Name	Default Value	Description
31:26		0	Reserved
25:24	RP	0h	Relative Performance
23:16	LBADS	Ch	LBA Data Size
15:00	MS	0h	Metadata Size

[Table 113] LBA Format 3 Data Structure

Bits	Name	Default Value	Description
31:26		0	Reserved
25:24	RP	2h	Relative Performance
23:16	LBADS	Ch	LBA Data Size (2^n bytes)
15:00	MS	8h	Metadata Size (bytes)

6.2 NVM Express I/O Command Set

[Table 114] Opcode for NVM Express I/O Commands

Opcode (Hex)	Command Name
00h	Flush
01h	Write
02h	Read
09h	Dataset Management

NOTE:
1) Deallocate feature in Dataset Management command is only supported in the Samsung SSD SZ1735.

7.0 SFF-8639 SMBus RESOURCES

This section listed data structures and registers accessible through SMBus interface.
Vital Product Data (VPD) is stored in SM-Bus slave address of 0xA6 (bits 7-1 correspond to 1010_011 on the SM-Bus). Temperature sensor is stored in SM-Bus slave address of 0xD4 (bits 7-1 correspond to 1101_010).

7.1 Vital Product Data (VPD) Structure

VPD listed device specific information for Enterprise PCIe SSD discovery and power allocation.

Bytes	Name	Default Value	Description
02:00	Class Code	010802h	Device Type & Programming Interface
04:03	ID	144Dh	PCI-SIG Vendor ID
24:05	ID	SXXXNXXXXXXXX	Serial Number (Vendor Unique, ASCII String), X: Variables
64:25	ID	800GB:MZWJJ800HMGQ-00007 1.6TB:MZWJJ1T6HMGG-00007 3.2TB:MZWJJ3T2HMHN-00007	Model Number (ASCII String)
65:65	PCIe Port 0 Capabilities	03h	Maximum Link Speed (PCIe Gen3)
66:66	PCIe Port 0 Capabilities	04h	Maximum Link Width (x8)
67:67	PCIe Port 1 Capabilities	03h	Maximum Link Speed (PCIe Gen3)
68:68	PCIe Port 1 Capabilities	04h	Maximum Link Width (x8)
69:69	Iniital Power Requirements	07h	12V Power rail initial power requirement (7 W)
71:70	Iniital Power Requirements	0h	Reserved
72:72	Max power Requirement	14h	12V Power rail maximum power requirement (20W)
74:73	Max power Requirement	0h	Reserved
76:75	Cap List Pointer	0050h	Start Cap Address Pointer (0x50)
79:77	-	0h	-
81:80	-	00A2h	VU Cap ID
83:82	-	0070h	Next Cap Address (0x0070 VU Samsung Specific)
84:84	Sensor Type	02h	-
85:85	Sensor Address	36h	-
87:86	-	0h	Reserved
88:88	Warning Thresh - LSB	E0h	-
89:89	Warning Thresh - MSB	04h	-
90:90	OverTemp Thresh - LSB	50h	-
91:91	OverTemp Thresh - MSB	05h	-
111:92	-	FFh	Reserved
113:112	-	00A0h	Dual Port Mode Capability
115:114	-	0074h	Next Cap Address (0x0074 Dual Active/Passive Capability)
117:116	-	00A3h	Dual Active/Passive Capability
119:118	-	0000h	Next Cap Address (NULL)
120:120	-	03h	Dual Port Vector (Dual Port Passive)
255:121	-	FFh	Reserved

NOTE: TSE2004av temperature encoding:

B15/B07	B14/B06	B13/B05	B12/B04	B11/B03	B10/B02	B09/B01	B08/B00
N/A	N/A	N/A	Sign	128	64	32	16
8	4	2	1	N/A	N/A	N/A	N/A

The 16-bit value is 2s complement representation of a temperature with the Bit 4 equal to the minimum granularity of 1 °C. Bit 12 is the sign bit.
For example:
1. a value of 0190h represents 25 °C,
2. a value of 07C0 h represents 124 °C, and
3. a value of 1E80 h represents –24 °C

By choosing the starting of the lowest bit the resolution of the temperature sensor can be defined. For SMBus temperature capability support PM1725's temperature sensor is at resolution of 1°C (8-bit)

7.2 Temperature Sensor Register Summary

Offset	Type	Name	Description	Default
00	RO	Capabilities	Indicates the functions and capabilities	0006h
01	RW	Configuration	Temperature sensor control	0000h
02	RW	High Limit	Temperature High Limit	0x04C0
03	RW	Low Limit	Temperature Low Limit	0
04	RW	TCRIT Limit	Critical Temperature	0x0530
05	RO	Ambient Temp	Current Ambient Temperature	N/A
06	RO	Manufacture ID	PCI-SIG Manufacture ID	144Dh
07	RO	Device/Revision	Device ID and Revision number	A821h

7.2.1 Capabilities Register

Bits	Type	Default Value	Description
15:07	RO	0	Reserved
6	RO	0	Bus timeout period for thermal sensor access during normal operation. 0 = timeout is supported in the range of 10 to 60 ms 1 = timeout is supported in the range of 25ms to 35 ms (SMBus Compatible)
5	RO	0	Reserved
04:03	RO	0	Reserved
2	RO	1	Range Width: 0 = The temperature monitor clamps values lower than 0 °C 1 = The temperature monitor can read temperatures below 0 °C and sets the sign bit appropriately)
1	RO	1	Accuracy: 0 = Accuracy ±2 °C over the active range and ±3 °C over the monitoring range (C-grade). 1 = High accuracy ±1 °C over the active range and ±2 °C over the monitoring range (B-grade)
0	RO	0	Event: 0 = The device does not support interrupt capabilities. 1 = The device supports interrupt capabilities.

7.2.2 Configuration Register

Bits	Type	Default Value	Description
15:11	RW	0	Reserved
10:09	RW	0	Hysteresis: Control the hysteresis that is applied to all limits 00 = Hysteresis is disabled 01 = Hysteresis is enabled at 2C 10 = Hysteresis is enabled at 3 °C 11 = Hysteresis is enabled at 6 °C
08:00	RW	0	Reserved

7.2.3 High Limit Register

Bits	Type	Default Value	Description
15:13	RW	0	Reserved
12	RW	0	Sign bit of the temperature
11	RW	0	128 degree Celsius
10	RW	1	64 degree Celsius
09	RW	0	32 degree Celsius
08	RW	0	16 degree Celsius
07	RW	1	8 degree Celsius
06	RW	0	4 degree Celsius
05	RW	1	2 degree Celsius
04	RW	0	1 degree Celsius
03:00	RW	0	Reserved

7.2.4 Low Limit Register

Bits	Type	Default Value	Description
15:13	RW	0	Reserved
12	RW	0	Sign bit of the temperature
11	RW	0	128 degree Celsius
10	RW	0	64 degree Celsius
09	RW	0	32 degree Celsius
08	RW	0	16 degree Celsius
07	RW	0	8 degree Celsius
06	RW	0	4 degree Celsius
05	RW	0	2 degree Celsius
04	RW	0	1 degree Celsius
03:00	RW	0	Reserved

7.2.5 Critical Temperature Register

Bits	Type	Default Value	Description
15:13	RW	0	Reserved
12	RW	0	Sign bit of the temperature
11	RW	0	128 degree Celsius
10	RW	1	64 degree Celsius
09	RW	0	32 degree Celsius
08	RW	1	16 degree Celsius
07	RW	0	8 degree Celsius
06	RW	0	4 degree Celsius
05	RW	0	2 degree Celsius
04	RW	0	1 degree Celsius
03:00	RW	0	Reserved

7.2.6 Ambient Temperature Register

Bits	Type	Default Value	Description
15	RO	0	TCRIT Flag: The temperature is above the TCRIT Limit.
14	RO	0	High Flag: The temperature is above the High Limit.
13	RO	0	Low Flag: The temperature is below the Low Limit.
12	RO	0	Sign bit of the temperature
11	RO	0	128 degree Celsius
10	RO	0	64 degree Celsius
09	RO	0	32 degree Celsius
08	RO	0	16 degree Celsius
07	RO	0	8 degree Celsius
06	RO	0	4 degree Celsius
05	RO	0	2 degree Celsius
04	RO	0	1 degree Celsius
03:00	RO	0	Reserved

7.2.7 Manufacture ID Register

Bits	Type	Default Value	Description
15:0	RO	144Dh	PCI-SIG Manufacture ID

7.2.8 Device/Revision Register

Bits	Type	Default Value	Description
15:0	RO	0xA821	Device ID and Revision Number

8.0 UEFI EXPANSION ROM

The expansion ROM integrated in Samsung SSD SZ1735 supports booting UEFI operating system installed on the drive, it complies to UEFI standard, which is specified in UEFI v2.5 Specification.

8.1 Basic Information

- IA32/x64 architecture support: x64 only
- Binary executable size < 64KB
- Platform BIOS requirement: EFI Specification Revision 2.31+, EFI Shell Version 1.0
- Number of Admin Submission Queue/Admin Completion Queue entries: 2
- Number of IO Queue entries: 2
- Maximum number of IO queues supported: 2
- Interrupt used: None

8.1.1 General Features

- Supports various operating systems booting in UEFI mode
- Ability to boot from large partition (over 2TB) with GUID Partition Table (GPT)
- Provides drive information via UEFI user interface (HII) in pre-boot environment (such as model number, firmware revision and drive capacity)
- Supports Secure Boot
- UEFI standard APIs supporting followings in pre-boot environment (EFI Shell):
. Basic block read/write access (produced API: EfiBlockIoProtocol)
. Driver health information (produced API: EfiDriverHealthProtocol)
. Drive diagnostic function (produced API: EfiDriverDiagnostics2Protocol)
. NVMHCI functions: GetLogPage, Firmware Download/Activate and Format (produced API: EfiFirmwareManagementProtocol and NvmExpressPassThruProtocol)

8.2 Supported Operating Systems

Index	Operating Systems bootable on SZ1735 drive
1	Windows Server 2008 R2 64-bit
2	Windows Server 2012 64-bit
3	Windows Server 2012 R2 64-bit
4	Windows Server 2016 64-bit
5	RHEL 6.4 (Kernel 2.6.32)
6	RHEL 6.5 (Kernel 2.6.32)
7	RHEL 6.6 (Kernel 2.6.32)
8	RHEL 7 (Kernel 3.10.0)
9	RHEL 7.1 (Kernel 3.10.0)
10	SLES 11 SP3 (Kernel 3.0.13)
11	SLES 12 (Kernel 3.12.28)

9.0 PRODUCT COMPLIANCE

9.1 Product Regulatory Compliance and Certifications

[Table 115] Certifications and Declarations

Category	Certifications
Safety	c-UL-us
	CE
	TUV-GS
	CB
EMC	CE (EU)
	BSMI (Taiwan)
	KC (South Korea)
	VCCI (Japan)
	Morocco (Morocco)
	RCM (Australia)
	FCC (USA) / IC (Canada)

The three existing compliance marks (C-Tick, A-Tick, and RCM) are consolidated into a single compliance mark - the RCM.

Caution: Any changes or modifications in construction of this device which are not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

NOTE:
This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications, However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:
- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio / TV technician for help.

Modifications not expressly approved by the manufacturer could void the user's authority to operated the equipment under FCC rules.

1. 기자재 명칭 : SSD (Solid State Drive)
2. 모델명(Model): 라벨 별도 표기
3. 제조연월 : 라벨 별도 표기
4. 제조자 : 삼성전자(주)
5. 제조국가 : 대한민국
6. 상호명 : 삼성전자(주)

Industry Canada ICES-003 Compliance Label:
CAN ICES-3 (B)/NMB-3(B)

10.0 REFERENCES

[Table 116] Standards References

Item	Website
PCI Express Base Specification Revision 3.0	http://www.pcisig.com/specifications/pciexpress/base3/
NVM Express Specification Rev. 1.2	http://www.nvmexpress.org/
Enterprise SSD Form Factor Version 1.0a	http://www.ssdformfactor.org/
Solid-State Drive Requirements and Endurance Test Method (JESD218A)	http://www.jedec.org/standards-documents/docs/jesd218a
Solid-State Drive Requirements and Endurance Test Method (JESD219A)	http://www.jedec.org/standards-documents/docs/jesd219a