2450 PCIe NVMe NAND Flash SSD

MTFDKBA256TFK, MTFDKBA512TFK, MTFDKBA1T0TFK, MTFDKCD256TFK, MTFDKCD512TFK, MTFDKCD1T0TFK, MTFDKBK256TFK, MTFDKBK512TFK, MTFDKBK1T0TFK

Features

- Micron® 3D TLC NAND Flash
- PCIe® Gen4 x4
- NVMe 1.4
  - Number of namespaces supported: 1
  - Weighted round robin with urgent priority class
  - Autonomous power state transitions
  - Host memory buffer(HMB)
- TCG/Pyrite 2.01 compliant non-self-encrypting drive (non-SED)
- TCG/Opal 2.01 compliant self-encrypting drive (SED)
  - Hardware-based AES-256 encryption engine
- Capacity (unformatted)[1]: 256GB, 512GB, 1024GB
- Endurance: Total bytes written (TBW)
  - Up to 600TB
- Industry-standard 512 byte sector size support
- Security
  - Digitally signed firmware
  - Secure boot support
  - Secure firmware download
- Self-monitoring, analysis, and reporting technology (SMART)
- Device self-test
- Power loss protection for data-at-rest
- Power loss signal support
- Performance[2]
  - Sequential 128KB READ: Up to 3600 MB/s
  - Sequential 128KB WRITE: Up to 3000 MB/s
  - Random 4KB READ: Up to 450,000 IOPS
  - Random 4KB WRITE: Up to 500,000 IOPS
- Latency[3]
  - Read (TYP): 50µs
  - Write (TYP): 12µs
- Reliability
  - MTTF: 2 million device hours[4]
  - Static and dynamic wear leveling
  - Uncorrectable bit error rate (UBER): <1 sector per 10^{15} bits read
- Low power consumption
  - Sleep/NVMe power state 4: <3mW
- Non-operating shock: 1500G/0.5ms
- Non-operating vibration: 5–3000Hz @ 20G
- Operating temperature[5]
  - Commercial (0°C to +70°C)
  - Host-controlled thermal management
  - System management bus temperature monitoring (SMBus)
- Micron redundant array of independent NAND (RAIN) technology
- Field upgradeable firmware
  - Firmware activation without reset
- Form factor
  - M.2 Type 2280
  - M.2 Type 2242
  - M.2 Type 2230
  - Single sided S3
- Electrical specification
  - Power supply: 3.3V ±5%

Supported Operating Systems

- Operating systems supported natively
  - Microsoft Windows® 10
  - Fedora® 33
  - Ubuntu® 20.10
  - CentOS® 8.2
  - Red Hat Enterprise Linux® 8.2
  - openSUSE® Leap 15.2
  - Debian® 10
  - Mint® 20
- Operating systems supported by a Micron Driver
  - Microsoft Windows® 10

Notes

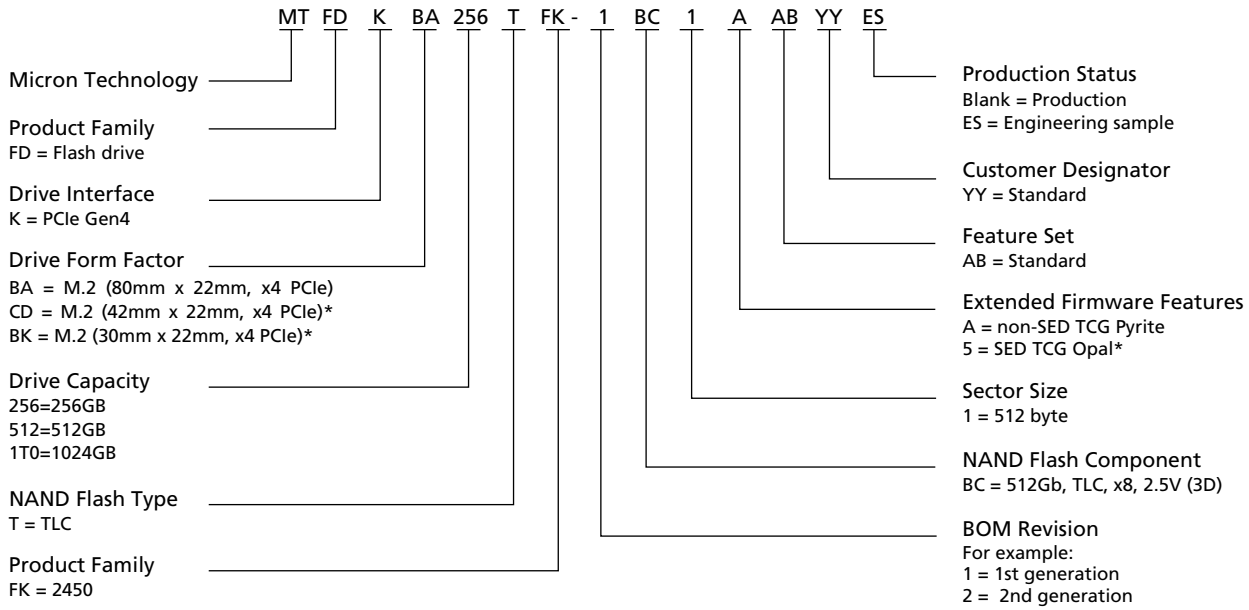
1. User capacity: 1GB = 1 billion bytes.
2. Typical I/O performance numbers as measured fresh-out-of-box (FOB).
3. 4KB, queue depth 1 transfers used for READ/WRITE latency values.
4. The product achieves a mean time to failure (MTTF) based on population statistics not relevant to individual units.
5. Temperature measured by SMART.

Warranty: Contact your Micron sales representative for further information regarding the product, including product warranties.

Part Numbering Information

Micron's 2450 SSD is available in different configurations and capacities. The chart below is a comprehensive list of options for the 2450 series devices; not all options listed can be combined to define an offered product. Visit www.micron.com for a list of valid part numbers.

Figure 1: Part Number Chart



Note * Contact your local Micron representative for details.

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General Description

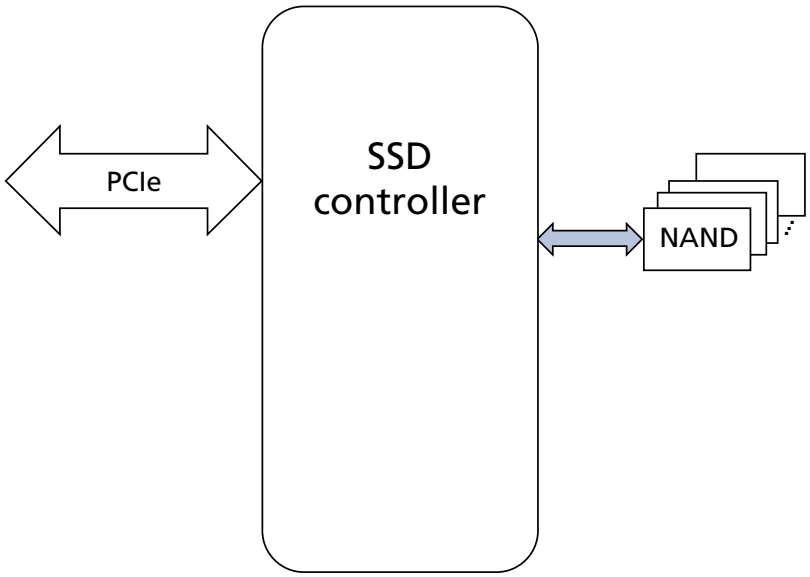
Micron's 2450 SSD uses a single-chip four-channel controller with a PCIe Gen4 interface connecting up to four PCIe lanes to Micron's 3D TLC NAND Flash. The 2450 is a DRAM-less design implementing the NVMe host memory buffer feature. The SSD is available in the M.2 2280 form factor.

The SSD is designed to use the PCIe interface efficiently during both READs and WRITEs while delivering bandwidth-focused, low latency performance through the innovative nonvolatile memory express protocol. SSD technology enables enhanced boot times, faster application load times, reduced power consumption, and extended reliability.

The non-self-encrypting drive (non-SED) provides data security through access control of the drive interface. The non-SED follows the TCG Pyrite specification for trusted peripherals.

The self-encrypting drive (SED) adds an AES-256 encryption engine providing hardware-based data encryption, with no loss of SSD performance. The SED follows the TCG Opal specification for trusted peripherals.

Figure 2: Functional Block Diagram



Performance

Measured performance can vary for a number of reasons. The major factors affecting drive performance are the capacity of the drive and the interface of the host. Additionally, overall system performance can affect the measured drive performance. When comparing drives, it is recommended that all system variables are the same, and only the drive being tested varies.

Performance numbers will vary depending on the host system configuration.

For SSDs designed for the client computing market, Micron specifies performance in fresh-out-of-box (FOB) state.

For a description of these performance states and of Micron's best practices for performance measurement, refer to Micron's technical marketing brief Best Practices for SSD Performance Measurement.

Table 1: PCIe Gen4 Drive Performance for 22x30 and 22x42 Form Factor

Gen 4 Parameter (22x30,22x42)	Capacity			Unit
	256GB	512GB	1024GB	
Sequential read (128KB transfer)	3000	3000	3000	MB/s
Sequential write (128KB transfer)	1600	3000	3000	MB/s
Random read (4KB transfer)	190,000	380,000	450,000	IOPS
Random write (4KB transfer)	400,000	500,000	500,000	IOPS
READ latency (TYP)	50	50	50	µs
WRITE latency (TYP)	12	12	12	µs

Table 2: PCIe Gen4 Drive Performance for 22x80 Form Factor

Gen4 Parameter (22x80)	Capacity			Unit
	256GB	512GB	1024GB	
Sequential read (128KB transfer)	3600	3600	3600	MB/s
Sequential write (128KB transfer)	1600	3000	3000	MB/s
Random read (4KB transfer)	190,000	380,000	450,000	IOPS
Random write (4KB transfer)	400,000	500,000	500,000	IOPS
READ latency (TYP)	50	50	50	µs
WRITE latency (TYP)	12	12	12	µs

Notes:

1. Performance values measured under the following conditions:
   - Fresh-out-of-box (FOB) state, unformatted
   - Drive write cache enabled
   - NVMe power state 0
   - Sequential workloads measured using FIO with a queue depth of 32
   - Random workloads measured using FIO with a queue depth of 128
   - HMB enabled
2. Performance values measured with the following system configuration:
   - ASRock® X570 Taichi Motherboard

- AMD® X570 Chipset
- AMD® Ryzen™ 7 3700X Processor
- Crucial® 16GB (2 x 8GB) DDR4-3600 SDRAM

3. Latency values measured under the following conditions:
   - Random workloads using FIO with 4KB transfers and a queue depth of 1
   - TYP = median, 50th percentile
4. System variations will affect measured results.
5. Performance and latency values applicable to both PCIe Gen3 and Gen4 link interfaces.

Logical Block Address Configuration

The drive is set to report the number of logical block addresses (LBA) that will ensure sufficient storage space for the specified capacity. Standard LBA settings, based on the IDEMA standard (LBA1-03), are shown below.

Table 3: Standard LBA Settings

Capacity	Total 512-Byte LBA		Max 512-Byte LBA		User Available Bytes
	Decimal	Hexadecimal	Decimal	Hexadecimal	(Unformatted)
256GB	500,118,192	1DCF32B0	500,118,191	1DCF32AF	256,060,514,304
512GB	1,000,215,216	3B9E12B0	1,000,215,215	3B9E12AF	512,110,190,592
1024GB	2,000,409,264	773BD2B0	2,000,409,263	773BD2AF	1,024,209,543,168

Reliability

The SSD incorporates advanced technology for defect and error management, using various combinations of hardware-based error correction algorithms and firmware-based static and dynamic wear-leveling algorithms.

Over the life of the SSD, uncorrectable errors may occur. An uncorrectable error is defined as data that is reported as successfully programmed to the SSD but when it is read out of the SSD, the data differs from what was programmed.

Table 4: Uncorrectable Bit Error Rate

Uncorrectable Bit Error Rate	Operation
<1 sector per 10^{15} bits read	READ

Mean Time To Failure

Mean time to failure (MTTF) for the SSD can be predicted based on the component reliability data using the methods referenced in the Telcordia SR-332 reliability prediction procedures for electronic equipment.

Table 5: MTTF

Capacity	MTTF (Operating Hours)
All capacities	2 million

Note: 1. The product achieves a mean time to failure (MTTF) of 2 million hours, based on population statistics not relevant to individual units.

Endurance

Endurance for the SSD can be predicted based on the usage conditions applied to the device, the internal NAND component cycles, the write amplification factor, and the wear-leveling efficiency of the drive. The tables below show the drive lifetime for each SSD capacity by client computing and sequential input and based on predefined usage conditions.

Table 6: Total Bytes Written

Capacity	Total Bytes Written
256GB	180TB
512GB	300TB
1024GB	600TB

Notes:
1. Total bytes written validated with the drive 90% full.
2. SSD volatile write cache is enabled.
3. Access patterns used during reliability testing are 25% sequential and 75% random and consist of the following: 1% are 512B; 24% are 4 KiB; 10% are 8 KiB; 10% are 16 KiB; 17% are 32 KiB; 18% are 64 KiB; 10% are 128 KiB; and 10% are 256 KiB.
4. Host workload parameters, including write cache settings, I/O alignment, transfer sizes, randomness, and percent full, that are substantially different than the described notes may result in varied endurance results.
5. GB/day can be estimated by dividing the total bytes written value by (365 × number of years). For example: 100TB/3 years/365 days = 91GB/day for 3 years.

Electrical Characteristics

Environmental conditions beyond those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 7: NVMe Power Consumption

	NVMe Power State							
	PS4	PS3	PS2	PS1	PS0			
Capacity	Sleep	Slumber	Heavy Throttle	Light Throttle	Active Idle	Active Writes*	Active Reads*	Unit
256GB	<3	<30	<1500	<3000	<400	<5500	<5500	mW
512GB	<3	<30	<1500	<3000	<400	<5500	<5500	mW
1024GB	<3	<30	<1500	<3000	<400	<5500	<5500	mW

Notes:
1. Active read power is a typical RMS active average power measurement performed using FIO with 128KB sequential read transfers.
2. Active write power is a typical RMS active average power measurement performed using FIO with 128KB sequential write transfers.
3. PS3 power measured at 25°C.
4. Power measurements applicable to both PCIe Gen3 and Gen4 link interfaces.
5. * For 2242 and 2230, Active Read/Write < 4300mW; 2280 <5500mW.

Table 8: Maximum Ratings

Parameter/Condition	Symbol	Min	Max	Unit
Voltage input	3.3V	3.135	3.465	V
Operating temperature[1]	T_C	0	70	°C
Non-operating temperature	–	–40	85	°C
Rate of temperature change	–	–	20	°C/hour
Relative humidity (non-condensing)	–	5	95	%

Notes:
1. Temperature measured by SMART.
2. If SMART temperature exceeds 70°C, performance will be throttled.

Table 9: Shock and Vibration

Parameter/Condition	Specification
Non-operating shock	1500G/0.5ms
Non-operating vibration	5–3000Hz @ 20G

Power Loss Signal Support

The 2450 SSD implements power loss signal support on the M.2 form factor where there is insufficient area to implement full power loss protection circuitry. This is accomplished through the addition of the power loss notification (PLN#) signal (electrical behavior defined in PLI_1.8V_USB_Higher Power ECN) which notifies the drive of an impending loss of power. Support for this feature is expected to be ratified in future releases of the PCIe and NVMe specifications.

Power Loss Procedure

1. Host asserts PLN#:
    a. Drive stops processing NVMe and SMBus commands, incoming commands are queued.
    b. Host data is saved to NAND, including host IO data that has been acknowledged and host IO commands that have been already fetched by firmware.
    c. DEALLOCATE - TRIM operations are paused.
    d. Power loss event is recorded to the PLN log.
    e. FTL tables are not flushed.
2. Host allows 2 seconds for the operation to complete before safely removing power.
    a. If PLN# is no longer asserted, then the drive resumes normal operation, paused DEALLOCATE - TRIM operations and queued command processing is restarted.
    b. Otherwise, the drive is powered-down (shutdown).

Power On Procedure

1. After power is applied, the drive boots as it would follow a dirty power cycle.
2. Drive queries the PLN log to determine if a PLN event occurred prior to the last shutdown. This information is used to optimize time-to-ready. Any paused DEALLOCATE - TRIM operations are restarted.

Logging

PLN events are recorded in the Persistent Event (Log Identifier 0Dh) and the Power Loss Notification (Log Identifier EFh). The logs contain the number of completed PLN events and incomplete PLN events as defined below:

- Complete PLN event: The power loss routine completed before power was removed or the PLN routine completed, and then the PLN signal is released with no power loss.
- Incomplete PLN event: Occurs when power is removed from the drive before the PLN routine is complete. This scenario is similar to a dirty power cycle in that the system is not aware the PLN was incomplete until power up. This case may occur if power is removed early or if the PLN routine takes longer than expected.

Table 10: Power Loss Notification (Log Identifier EFh)

Bytes	PLN Log Description
31:8	Reserved
7:4	Accumulated count of incomplete PLN events
3:0	Accumulated count of completed PLN events

Additional PLN Considerations

- PLN is ignored while PERST# is asserted. If PERST# is asserted while PLN is processing, firmware finishes the PLN process and then process PERST#.
- PLN is ignored while the drive is in NVMe power states 3 (PS3) and 4 (PS4). Loss of power is treated normally and the PLN log is not updated.
- PLN is ignored while CSTS.RDY is reset. If PLN is asserted when CSTS.RDY becomes set, then the PLN process is executed.

Power Loss Notification Set/Get Features

PLN SET/GET FEATURES commands adhere to the standard commands defined by the NVMe specification.

Table 11: PLN Get Features Completion Response for Current, Default, and Saved Select Fields

Power Loss Signal Support Get Features Admin Command Op Code = 0Ah, Feature ID = D0h

DWORD	Bit	Definition	Function
0	31:8	Reserved	–
	7:4	PLN Pulse Width	In 10ms units
	3	Reserved	–
	2	Emergency Power Fail	1 = selected (Fixed)
	1	Forced Quiescence	0 = not supported
	0	PLN	1 = Enabled 0 = Disabled (default)

Table 12: PLN Get Features Completion Response for Supported Capabilities Select Field

Power Loss Signal Support Get Features Admin Command Op Code = 0Ah, Feature ID = D0h

DWORD	Bit	Definition	Function
0	31:3	Reserved	–
	2	Changeable	1 = PLN is changeable
	1	Namespace specific	0 = PLN is not namespace specific
	0	Savable	1 = PLN is savable

Table 13: PLN Set Features Configuration Command

Power Loss Signal Support Set Features Admin Command Op Code = 09h, Feature ID = D0h

DWORD	Bit	Definition	Function
10	31	SV (Save)	SV = 1 PLN is persistent SV = 0 PLN is not persistent
	30:8	Reserved	–
	7:0	Feature ID	D0h

Table 13: PLN Set Features Configuration Command (Continued)

Power Loss Signal Support Set Features Admin Command Op Code = 09h, Feature ID = D0h

DWORD	Bit	Definition	Function
11	31:8	Reserved	–
	7:4	PLN pulse width	In 10ms units, default = 50ms
	3	Reserved	–
	2	Emergency power fail	1 = selected (fixed)
	1	Forced quiescence	0 = not supported
	0	PLN	1 = to enable 0 = to disable

TCG Pyrite and Opal Support

Table 14: TCG Pyrite and Opal Support Parameters

Property	Support	Comment
TCG Pyrite Storage Specifications		
TCG Storage Security Subsystem Class: Pyrite Specification	Version 2.01	Revision 1.00
TCG Storage Interface Interactions Specification	Version 1.08	Revision 1.00
TCG Storage Architecture Core Specification	Version 2.01	Revision 1.00
TCG Storage Security SubSystem Class: Opal Specification	Version 2.01	Revision 1.00
TCG Storage Feature Set: Block SID Authentication	Version 1.00	Revision 1.00
TCG Pyrite SSC Features		
Number of Locking SP Admin Authorities supported	2	
Number of Locking SP User Authorities supported	2	
TCG Opal Storage Specifications		
TCG Storage Security SubSystem Class: Opal Specification	Version 2.01	Revision 1.00
TCG Storage Interface Interactions Specification	Version 1.04	Revision 1.00
TCG Storage Architecture Core Specification	Version 2.01	Revision 1.00
Additional Data Store (ADS) Specification	Version 1.00	Revision 1.00
TCG Storage Opal SSC Feature Set: PSID Specification	Version 1.00	Revision 1.00
TCG Storage Feature Set: Block SID Authentication	Version 1.00	Revision 1.00
NIST, FIPS-197, 2001, "Advanced Encryption Standard (AES)"		
TCG Storage Security SubSystem Class: Opal Specification 1.00	Not supported	Not backward compatible
TCG Opal SSC Features		
Number of Locking SP Admin Authorities supported	4	
Number of Locking SP User Authorities supported	9	
Cryptographic Features		
AES key size	256 bits	
User data encryption algorithm	XTS-AES	
Asymmetric Verification Key Size	2048	
Asymmetric Verification Encryption Algorithm	RSA	
Verification Key Usage	Supported	
Number of Ranges/Band Supported	9 maximum	
NIST Cryptographic Algorithm Certification	Certifiable	
Secure Encryption Bypass Support	Supported	

Identify – Identify Controller Data Structure

Table 15: Identify – Identify Controller Data Structure

Bytes	Default Value	Description
01:00	1344h	**PCI Vendor ID (VID):** Contains the Micron identifier assigned by the PCI SIG.
03:02	1344h	**PCI Subsystem Vendor ID (SSVID):** Contains the Micron identifier assigned by the PCI SIG for the subsystem.
23:04	Variable	**Serial Number (SN):** Contains the serial number for the NVM subsystem as an ASCII string.
63:24	Variable	**Model Number (MN):** Contains the model number for the NVM subsystem as an ASCII string.
71:64	Variable	**Firmware Revision (FR):** Contains the currently active firmware revision for the NVM subsystem.
72	6	**Recommended Arbitration Burst (RAB):** This is the recommended arbitration burst size.
75:73	00A075h	**IEEE OUI Identifier (IEEE):** Contains the organization unique identifier (OUI).
76	0	**Controller Multi-Path I/O and Namespace Sharing Capabilities (CMIC):** This field specifies multi-path I/O and namespace sharing capabilities of the controller and NVM subsystem. Bits 7:3 are reserved Bit 2 = 0 the controller is associated with a PCI function Bit 1 = 0 the NVM subsystem contains only a single controller Bit 0 = 0 the NVM subsystem contains only a single PCI Express port
77	6	**Maximum Data Transfer Size (MDTS):** This field indicates the maximum data transfer size between the host and the controller. The host should not submit a command that exceeds this transfer size. If a command is submitted that exceeds the transfer size, then the command is aborted with a status of Invalid Field in command. The value is in units of the minimum memory page size (4096 bytes) and is reported as a power of two (2^n).
79:78	0	**Controller ID (CNTLID):** Contains the NVM subsystem unique controller identifier associated with the controller.
83:80	00010400h	**Version (VER):** This register indicates the major and minor version of the NVM Express specification that the controller implementation supports.
87:84	7A120h	**RTD3 Resume Latency (RTD3R):** This field indicates the typical latency in microseconds resuming from Runtime D3 (RTD3).
91:88	4C4B40h	**RTD3 Entry Latency (RTD3E):** This field indicates the typical latency in microseconds to enter Runtime D3 (RTD3).

Table 15: Identify – Identify Controller Data Structure (Continued)

Bytes	Default Value	Description
95:92	0200h	**Optional Asynchronous Events Supported (OAES):** This field indicates the optional asynchronous events supported by the controller. A controller shall not send optional asynchronous events before they are enabled by host software. Bits 31:15 are reserved Bit 14 = 0 the controller does not support the Endurance Group Event Aggregate Log Page Change Notices event Bit 13 = 0 the controller does not support the LBA Status Information Notices event Bit 12 = 0 the controller does not support the Predictable Latency Event Aggregate Log Change Notices event Bit 11 = 0 the controller does not support the Asymmetric Namespace Access Change Notices event Bit 10 is reserved Bit 9 = 1 the controller supports sending Firmware Activation Notices Bit 8 = 0 the controller does not support the Namespace Attribute Changed event Bits 7:0 are reserved
99:96	2	**Controller Attributes (CTRATT):** This field indicates attributes of the controller. Bits 31:10 are reserved Bit 9 = 0 the controller does not support reporting of a UUID List Bit 8 = 0 the controller does not support SQ Associations Bit 7 = 0 the controller does not support reporting of Namespace Granularity Bit 6 = 0 the controller does not support Traffic Based Keep Alive Support Bit 5 = 0 the controller does not support Predictable Latency Mode Bit 4 = 0 the controller does not support Endurance Groups Bit 3 = 0 the controller does not support Read Recovery Levels Bit 2 = 0 the controller does not support NVM Sets Bit 1 = 1 the controller supports non-operational power state permissive mode where the controller may temporarily exceed the power of a non-operational power state for the purpose of executing controller initiated background operations in a non-operational power state Bit 0 = 0 the controller does not support a 128-bit Host Identifier
101:100	0	**Read Recovery Levels Supported (RRLS):** Read Recovery Levels are not supported.
110:102	–	Reserved
111	1	**Controller Type (CNTRLTYPE):** This field specifies the controller type. 1h = I/O Controller
127:112	0	**FRU Globally Unique Identifier (FGUID):** FRU Globally Unique Identifier is not supported.
129:128	0	**Command Retry Delay Time 1 (CRDT1):** Command Retry Delay Time 1 is not supported.
131:130	0	**Command Retry Delay Time 2 (CRDT2):** Command Retry Delay Time 2 is not supported.
133:132	0	**Command Retry Delay Time 3 (CRDT3):** Command Retry Delay Time 3 is not supported
239:134	–	Reserved

Table 15: Identify – Identify Controller Data Structure (Continued)

Bytes	Default Value	Description
255:240	0	**NVMe Management Interface:** NVMe Management Interface is not supported.
257:256	0000000000010111b	**Optional Admin Command Support (OACS):** This field indicates the optional Admin commands supported by the controller. Bits 15:10 are reserved Bit 9 = 0 the controller does not support the Get LBA Status capability Bit 8 = 0 the controller does not support the DOORBELL BUFFER CONFIG command Bit 7 = 0 the controller does not support the VIRTUALIZATION MANAGEMENT command Bit 6 = 0 the controller does not support the NVMe-MI SEND and NVMe-MI RECEIVE commands Bit 5 = 0 the controller does not support DIRECTIVES Bit 4 = 1 the controller supports the DEVICE SELF TEST (DST) command Bit 3 = 0 the controller does not support the NAMESPACE MANAGEMENT and NAMESPACE ATTACHMENT commands Bit 2 = 1 the controller supports the FIRMWARE COMMIT and FIRMWARE IMAGE DOWNLOAD commands Bit 1 = 1 the controller supports the FORMAT NVM command Bit 0 = 1 the controller supports the SECURITY SEND and SECURITY RECEIVE commands
258	3h	**Abort Command Limit (ACL):** This field is used to convey the maximum number of concurrently outstanding ABORT commands supported by the controller. This is a 0's based value.
259	7h	**Asynchronous Event Request Limit (AERL):** This field is used to convey the maximum number of concurrently outstanding ASYNCHRONOUS EVENT REQUEST commands supported by the controller. This is a 0's based value.
260	00010100b	**Firmware Updates (FRMW):** This field indicates capabilities regarding firmware updates. Bits 7:5 are reserved Bit 4 = 1 the controller supports firmware activation without a reset Bits 3:1 = 010 the number of firmware slots that the controller supports Bit 0 = 0 the first firmware slot (slot 1) is read/write
261	00011110b	**Log Page Attributes (LPA):** This field indicates optional attributes for log pages that are accessed via the GET LOG PAGE command. Bits 7:5 are reserved Bit 4 = 1 the controller supports the Persistent Event log Bit 3 = 1 the controller supports the Telemetry Host-Initiated and Telemetry Controller-Initiated log pages and sending Telemetry Log Notices Bit 2 = 1 the controller supports extended data for the Get log page Bit 1 = 1 the controller supports the Command Effects log page Bit 0 = 0 the controller does not support the SMART/Health Information log page on a per namespace basis
262	62h	**Error Log Page Entries (ELPE):** This field indicates the number of Error Information log entries that are stored by the controller. This field is a 0's based value.
263	4h	**Number of Power States Support (NPSS):** This field indicates the number of NVM Express power states supported by the controller. This is a 0's based value.

Table 15: Identify – Identify Controller Data Structure (Continued)

Bytes	Default Value	Description
264	1	**Admin Vendor Specific Command Configuration (AVSCC):** This field indicates the configuration settings for Admin Vendor Specific command handling. Bits 7:1 are reserved Bit 0 = 1 Admin Vendor Specific Commands use the format defined in the NVMe specification
265	00000001b	**Autonomous Power State Transition Attributes (APSTA):** This field indicates the attributes of the autonomous power state transition feature. Bits 7:1 are reserved Bit 0 = 1 the controller supports autonomous power state transitions
267:266	164h	**Warning Composite Temperature Threshold (WCTEMP):** This field indicates the minimum Composite Temperature field value (Temperature value reported in the SMART/Health Information log) that indicates an overheating condition during which controller operation continues. Immediate remediation is recommended (for example, additional cooling or workload reduction). The platform should strive to maintain a composite temperature below this value.
269:268	166h	**Critical Composite Temperature Threshold (CCTEMP):** This field indicates the minimum Composite Temperature field value (Temperature value reported in the SMART/Health Information log) that indicates a critical overheating condition (for example, automatic device shutdown).
271:270	32h	**Maximum Time for Firmware Activation (MTFA):** Indicates the maximum time the controller temporarily stops processing commands to activate the firmware image. This field is specified in 100 millisecond units.
275:272	16384	**Host Memory Buffer Preferred Size (HMPRE):** This field indicates the preferred size that the host is requested to allocate for the Host Memory Buffer feature in 4 KiB units.
279:276	16384	**Host Memory Buffer Minimum Size (HMMIN):** This field indicates the minimum size that the host is requested to allocate for the Host Memory Buffer feature in 4 KiB units.
295:280	Variable	**Total NVM Capacity (TNVMCAP):** This field indicates the total NVM capacity in the NVM subsystem. The value is in bytes.
311:296	Variable	**Unallocated NVM Capacity (UNVMCAP):** This field indicates the unallocated NVM capacity in the NVM subsystem. The value is in bytes.
315:312	0	**Replay Protected Memory Block Support (RPMBS):** Replay Protected Memory Blocks is not supported.
317:316	1Eh	**Extended Device Self-test Time (EDSTT):** This field indicates the nominal amount of time in one minute units that the controller takes to complete an extended DEVICE SELF-TEST operation when in power state 0.
318	1	**Device Self-test Options (DSTO):** This field indicates the controller supports one DEVICE SELF TEST operation in progress at a time.
319	4	**Firmware Update Granularity (FWUG):** This field indicates the granularity and alignment requirement of the firmware image being updated by the FIRMWARE IMAGE DOWNLOAD command.
321:320	0	**Keep Alive Support (KAS):** Keep Alive is not supported.

Table 15: Identify – Identify Controller Data Structure (Continued)

Bytes	Default Value	Description
323:322	1	**Host Controlled Thermal Management Attributes (HCTMA):** This field indicates the attributes of the host controlled thermal management feature. Bits 15:1 are reserved Bit 0 = 1 the controller supports host controlled thermal management
325:324	273	**Minimum Thermal Management Temperature (MNTMT):** This field indicates the minimum temperature, in degrees Kelvin, that the host may request in the Thermal Management Temperature 1 field and Thermal Management Temperature 2 field of a SET FEATURES command.
327:326	358	**Maximum Thermal Management Temperature (MXTMT):** This field indicates the maximum temperature, in degrees Kelvin, that the host may request in the Thermal Management Temperature 1 field and Thermal Management Temperature 2 field of a SET FEATURES command.
331:328	Variable	**Sanitize Capabilities (SANICAP):** This field indicates attributes for sanitize operations. Bits 31:3 are reserved Bit 2 = 0 the controller does not support the OVERWRITE SANITIZE operation Bit 1 = 1 the controller supports the BLOCK ERASE SANITIZE operation Bit 0 = Variable. 1 indicates CRYPTO ERASE SANITIZE operation is supported for the SED product variant. 0 indicates CRYPTO ERASE SANITIZE operation is not supported for the non-SED product variant.
335:332	1024	**Host Memory Buffer Minimum Descriptor Entry Size (HMMINDS):** This field indicates the minimum usable size of a Host Memory Buffer Descriptor Entry in 4 KiB units.
337:336	16	**Host Memory Maximum Descriptors Entries (HMMAXD):** This field indicates the number of usable Host Memory Buffer Descriptor Entries.
339:338	0	**NVM Set Identifier Maximum (NSETIDMAX):** NVM Set Identifier Maximum is not supported.
341:340	0	**Endurance Group Identifier Maximum (ENDGIDMAX):** Endurance Group Identifier Maximum is not supported.
342	0	**ANA Transition Time (ANATT):** ANA Transition Time is not supported.
343	0	**Asymmetric Namespace Access Capabilities (ANACAP):** Asymmetric Namespace Access Capabilities is not supported.
347:344	0	**ANA Group Identifier Maximum (ANAGRPMAX):** ANA Group Identifier Maximum is not supported.
351:348	0	**Number of ANA Group Identifiers (NANAGRPID):** Number of ANA Group Identifiers is not supported.
355:352	125	**Persistent Event Log Size (PELS):** This field indicates the maximum reportable size for the Persistent Event Log in 64 KiB units.
511:356	–	Reserved

Table 15: Identify – Identify Controller Data Structure (Continued)

Bytes	Default Value	Description
512	66h	**Submission Queue Entry Size (SQES):** This field defines the required and maximum submission queue entry size when using the NVM command set. Bits 7:4 = 6 defines the maximum submission queue entry size when using the NVM command set. The value is in bytes and is reported as a power of two (2^n). Bits 3:0 = 6 defines the required submission queue entry size when using the NVM command set. The value is in bytes and is reported as a power of two (2^n).
513	44h	**Completion Queue Entry Size (CQES):** This field defines the required and maximum completion queue entry size when using the NVM command set. Bits 7:4 = 4 defines the maximum completion queue entry size when using the NVM command set. The value is in bytes and is reported as a power of two (2^n). Bits 3:0 = 4 defines the required completion queue entry size when using the NVM command set. The value is in bytes and is reported as a power of two (2^n).
515:514	256	**Maximum Outstanding Commands (MAXCMD):** This field indicates the maximum number of commands that the controller processes at one time for a particular queue.
519:516	1	**Number of Namespaces (NN):** This field defines the number of valid namespaces present for the controller.
521:520	0000000001011111b	**Optional NVM Command Support (ONCS):** This field indicates the optional NVM commands and features supported by the controller. Bits 15:8 are reserved Bit 7 = 0 the controller does not support the Verify command Bit 6 = 1 the controller supports the Timestamp feature Bit 5 = 0 the controller does not support reservations Bit 4 = 1 the controller supports the save field in the SET FEATURES command and the select field in the GET FEATURES command Bit 3 = 1 the controller supports the WRITE ZEROS command Bit 2 = 1 the controller supports the DATASET MANAGEMENT command Bit 1 = 1 the controller supports the WRITE UNCORRECTABLE command Bit 0 = 1 the controller supports the COMPARE command
523:522	0	**Fused Operation Support (FUSES):** Fused Operation is not supported.
524	00000V00b	**Format NVM Attributes (FNA):** This field indicates attributes for the FORMAT NVM command. Bits 7:3 are reserved Bit 2 = Variable. 1 indicates cryptographic erase is supported as part of the secure erase functionality for the SED product variant. 0 indicates cryptographic erase is not supported as part of the secure erase functionality for the non-SED product variant. Bit 1 = 0 secure erase performed as part of a format results in a secure erase of the particular namespace specified Bit 0 = 0 the controller supports format on a per namespace basis

Table 15: Identify – Identify Controller Data Structure (Continued)

Bytes	Default Value	Description
525	00000111b	**Volatile Write Cache (VWC):** This field indicates attributes related to the presence of a volatile write cache in the implementation. Bits 7:3 are reserved Bits 2:1 = 11 Flush command supports the NSID field set to FFFFFFFFh Bit 0 = 1 volatile write cache is present. The host may issue FLUSH commands and control whether the volatile write cache is enabled with SET FEATURES specifying the volatile write cache feature identifier.
527:526	255	**Atomic Write Unit Normal (AWUN):** This field indicates the size of the WRITE operation guaranteed to be written atomically to the NVM with any supported namespace format during normal operation. This field is specified in logical blocks and is a 0's based value. If a WRITE command is submitted with size less than or equal to the AWUN value, the host is guaranteed that the WRITE command is atomic to the NVM with respect to other READ or WRITE commands. If a WRITE command is submitted with size greater than the AWUN value, then there is no guarantee of command atomicity. AWUN does not have any applicability to write errors caused by power failure (refer to Atomic Write Unit Power Fail).
529:528	0	**Atomic Write Unit Power Fail (AWUPF):** Atomic Write Unit Power Fail is not supported.
530	1	**NVM Vendor Specific Command Configuration (NVSCC):** This field indicates the configuration settings for NVM Vendor Specific command handling Bits 7:1 are reserved Bit 0 = 1 NVM Vendor Specific Commands use the format defined in the NVMe specification
531	0	**Namespace Write Protection Capabilities (NWPC):** This field indicates the optional namespace write protection capabilities supported by the controller Bits 7:3 are reserved Bit 2 = 0 the controller does not support the Permanent Write Protect state Bit 1 = 0 the controller does not support Write Protect Until Power Cycle state Bit 0 = 0 the controller does not support Namespace Write Protection
533:532	0	**Atomic Compare & Write Unit (ACWU):** Atomic Compare & Write Unit is not supported.
535:534	–	Reserved
539:536	0	**SGL Support (SGLS):** SGL is not supported.
543:540	0	**Maximum Number of Allowed Namespaces (MNAN):** This field indicates the maximum number of namespaces supported by the NVM subsystem. The maximum number of namespaces supported by the NVM subsystem is less than or equal to the value in the NN field.
767:544	–	Reserved
1023:768	Variable	**NVM Subsystem NVMe Qualified Name (SUBNQN):** This field specifies the NVM Subsystem NVMe Qualified Name as a UTF-8 null-terminated string.
2047:1024	–	Reserved
2079:2048	00000000000000000000000000000226h	**Power State 0 Descriptor (PSD0):** This field indicates the characteristics of power state 0.

Table 15: Identify – Identify Controller Data Structure (Continued)

Bytes	Default Value	Description
2111:2080	10101010000000000000000000000f0h	**Power State 1 Descriptor (PSD1):** This field indicates the characteristics of power state 1.
2143:2112	20202020000000000000000000000C0h	**Power State 2 Descriptor (PSD2):** This field indicates the characteristics of power state 2.
2175:2144	3030303000003e80000003E80030002bCh	**Power State 3 Descriptor (PSD3):** This field indicates the characteristics of power state 3.
2207:2176	404040400009C400000271003000032h	**Power State 4 Descriptor (PSD4):** This field indicates the characteristics of power state 4.
4095:2208	–	Reserved

Table 16: Identify - Identify Namespace Data Structure

Bytes	Default Value	Description
07:00	Variable	**Namespace Size (NSZE):** This field indicates the total size of the namespace in logical blocks. A namespace of size n consists of LBA 0 through (n - 1). The number of logical blocks is based on the formatted LBA size.
15:08	Variable	**Namespace Capacity (NCAP):** This field indicates the maximum number of logical blocks that may be allocated in the namespace at any point in time. The number of logical blocks is based on the formatted LBA size. A logical block is allocated when it is written with a WRITE or WRITE UNCORRECTABLE command. A logical block may be deallocated using the DATA-SET MANAGEMENT command.
23:16	Variable	**Namespace Utilization (NUSE):** This field indicates the current number of logical blocks allocated in the namespace. This field is equal to the Namespace Capacity. The number of logical blocks is based on the formatted LBA size. When using the NVM command set: A logical block is allocated when it is written with a WRITE or WRITE UNCORRECTABLE command. A logical block may be deallocated using the DATASET MANAGEMENT command.
24	0	**Namespace Features (NSFEAT):** This field defines features of the namespace. Bits 7:4 are reserved Bit 3 = 0 the NGUID value may be reused and the EUI64 value may be reused by the controller Bit 2 = 0 the controller does not support the Deallocated or Unwritten Logical Block error Bit 1 = 0 the controller does not support the fields NAWUN, NAWUPF, and NACWU for the namespace Bit 0 = 0 thin provisioning is not supported, the Namespace Size and Namespace Capacity fields report the same value
25	0	**Number of LBA Formats (NLBAF):** This field defines the number of supported LBA data sizes supported by the namespace. This is a 0's based value.
26	0	**Formatted LBA Size (FLBAS):** This field indicates the LBA data size that the namespace has been formatted with. Bits 7:5 are reserved Bit 4 = 0 the controller does not support metadata Bits 3:0 = 0 indicates a single supported LBA format
27	0	**Metadata Capabilities (MC):** Metadata Capabilities is not supported.

Table 16: Identify - Identify Namespace Data Structure (Continued)

Bytes	Default Value	Description
28	0	**End-to-end Data Protection Capabilities (DPC):** End-to-end Data Protection Capabilities is not supported.
29	0	**End-to-end Data Protection Type Settings (DPS):** End-to-end Data Protection Type Settings is not supported.
30	0	**Namespace Multi-path I/O and Namespace Sharing Capabilities (NMIC):** Namespace Multi-path I/O and Namespace Sharing Capabilities is not supported.
31	0	**Reservation Capabilities (RESCAP):** Reservation Capabilities field is not supported.
32	1VVVVVVVb	**Format Progress Indicator (FPI):** If a format operation is in progress, this field indicates the percentage of the namespace that remains to be formatted. Bit 7 = 1 the namespace supports the Format Progress Indicator defined by bits 6:0 in this field. Bits 6:0 = Variable. Indicates the percentage of the namespace that remains to be formatted (For example, a value of 25 indicates that 75% of the namespace has been formatted and 25% remains to be formatted). A value of 0 indicates that the namespace is formatted with the format specified by the FLBAS field in this data structure.
33	1	**Deallocate Logical Block Features (DLFEAT):** This field indicates information about features that affect deallocating logical blocks for this namespace. Bits 7:5 are reserved Bit 4 = 0 the Guard field for the deallocated logical blocks that contain protection information is set to FFFFh Bit 3 = 0 the controller does not support the Deallocate bit in the WRITE ZEROES command for this namespace Bits 2:0 = 001 the values read from a deallocated logical block and its metadata are cleared to 00h
35:34	0	**Namespace Atomic Write Unit Normal (NAWUN):** Namespace Atomic Write Unit Normal is not supported.
37:36	0	**Namespace Atomic Write Unit Power Fail (NAWUPF):** Namespace Atomic Write Unit Power Fail is not supported.
39:38	0	**Namespace Atomic Compare & Write Unit (NACWU):** Namespace Atomic Compare & Write Unit is not supported.
41:40	0	**Namespace Atomic Boundary Size Normal (NABSN):** Namespace Atomic Boundary Size Normal is not supported.
43:42	0	**Namespace Atomic Boundary Offset (NABO):** Namespace Atomic Boundary Offset is not supported.
45:44	0	**Namespace Atomic Boundary Size Power Fail (NABSPF):** Namespace Atomic Boundary Size Power Fail is not supported.
47:46	0	**Namespace Optimal I/O Boundary (NOIOB):** Namespace Optimal I/O Boundary is not supported.
63:48	Variable	**NVM Capacity (NVMCAP):** This field indicates the total size of the NVM allocated to this namespace. The value is in bytes.
65:64	0	**Namespace Preferred Write Granularity (NPWG):** Namespace Preferred Write Granularity is not supported.
67:66	0	**Namespace Preferred Write Alignment (NPWA):** Namespace Preferred Write Alignment is not supported.

Table 16: Identify - Identify Namespace Data Structure (Continued)

Bytes	Default Value	Description
69:68	0	**Namespace Preferred Deallocate Granularity (NPDG):** Namespace Preferred Deallocate Granularity is not supported.
71:70	0	**Namespace Preferred Deallocate Alignment (NPDA):** Namespace Preferred Deallocate Alignment is not supported.
73:72	0	**Namespace Optimal Write Size (NOWS):** Namespace Optimal Write Size is not supported.
91:74	–	Reserved
95:92	0	**ANA Group Identifier (ANAGRPID):** Asymmetric Namespace Access Reporting is not supported.
98:96	–	Reserved
99	Variable	**Namespace Attributes (NSATTR):** This field specifies attributes of the namespace. Bits 7:1 are reserved Bit 0: Variable. 1 indicates the namespace is currently write protected and all write access to the namespace shall fail. 0 indicates the namespace is not currently write protected.
101:100	0	**NVM Set Identifier (NVMSETID):** NVM Sets are not supported.
103:102	0	**Endurance Group Identifier (ENDGID):** Endurance Groups are not supported.
119:104	Variable	**Namespace Globally Unique Identifier (NGUID):** This field contains the 128-bit Namespace Globally Unique Identifier value.
127:120	Variable	**IEEE Extended Unique Identifier (EUI64):** This field contains the 64-bit IEEE Extended Unique Identifier value.
131:128	00090000h	**LBA Format 0 Support (LBAF0):** This field indicates the LBA format 0 that is supported by the controller. Bits 31:26 are reserved Bits 25:24 = 0 relative performance of the LBA format is not supported Bits 23:16 = 09 indicates the LBA data size supported, the value is reported in terms of a power of two (2^n) = 512 byte LBA data size Bits 15:0 = 0 metadata is not supported
4095:132	–	Reserved

Commands

Table 17: Op Codes for Admin Commands

Codes not listed are reserved. All commands in the table are supported.

Command Name	Op Code (hex)
DELETE I/O SUBMISSION QUEUE	00h
CREATE I/O SUBMISSION QUEUE	01h
GET LOG PAGE	02h
DELETE I/O COMPLETION QUEUE	04h
CREATE I/O COMPLETION QUEUE	05h
IDENTIFY	06h
ABORT	08h
SET FEATURES - SET ARBITRATION	09h - 01h
SET FEATURES - SET POWER MANAGEMENT	09h - 02h
SET FEATURES - SET LBA RANGE TYPE	09h - 03h
SET FEATURES - SET TEMPERATURE THRESHOLD	09h - 04h
SET FEATURES - SET ERROR RECOVERY	09h - 05h
SET FEATURES - SET VOLATILE WRITE CACHE	09h - 06h
SET FEATURES - SET NUMBER OF QUEUES	09h - 07h
SET FEATURES - SET INTERRUPT COALESCE	09h - 08h
SET FEATURES - SET INTERRUPT VECTOR CONFIGURATION	09h - 09h
SET FEATURES - SET WRITE ATOMICITY	09h - 0Ah
SET FEATURES - SET ASYNC EVENT CONFIGURATION	09h - 0Bh
SET FEATURES - SET AUTONOMOUS POWER STATE TRANSITION	09h - 0Ch
SET FEATURES - TIMESTAMP	09h - 0Eh
SET FEATURES - HOST CONTROLLED THERMAL MANAGEMENT	09h - 10h
SET FEATURES - NON-OPERATIONAL POWER STATE CONFIG	09h - 11h
SET FEATURES - POWER LOSS SIGNAL SUPPORT	09h - D0h
GET FEATURES - GET ARBITRATION	0Ah - 01h
GET FEATURES - GET POWER MANAGEMENT	0Ah - 02h
GET FEATURES - GET LBA RANGE TYPE	0Ah - 03h
GET FEATURES - GET TEMPERATURE THRESHOLD	0Ah - 04h
GET FEATURES - GET ERROR RECOVERY	0Ah - 05h
GET FEATURES - GET VOLATILE WRITE CACHE	0Ah - 06h
GET FEATURES - GET NUMBER OF QUEUES	0Ah - 07h
GET FEATURES - GET INTERRUPT COALESCE	0Ah - 08h
GET FEATURES - GET INTERRUPT VECTOR CONFIGURATION	0Ah - 09h
GET FEATURES - GET WRITE ATOMICITY	0Ah - 0Ah
GET FEATURES - GET ASYNC EVENT CONFIGURATION	0Ah - 0Bh
GET FEATURES - SET AUTONOMOUS POWER STATE TRANSITION	0Ah - 0Ch
GET FEATURES - TIMESTAMP	0Ah - 0Eh

Table 17: Op Codes for Admin Commands (Continued)

Codes not listed are reserved. All commands in the table are supported.

Command Name	Op Code (hex)
GET FEATURES - HOST CONTROLLED THERMAL MANAGEMENT	0Ah - 10h
GET FEATURES - NON-OPERATIONAL POWER STATE CONFIG	0Ah - 11h
GET FEATURES - POWER LOSS SIGNAL SUPPORT	0Ah - D0h
ASYNCHRONOUS EVENT REQUEST	0Ch
FIRMWARE COMMIT	10h
FIRMWARE IMAGE DOWNLOAD	11h
DEVICE SELF TEST (DST)	14h
FORMAT NVM	80h
SECURITY SEND	81h
SECURITY RECEIVE	82h
SANITIZE - BLOCK ERASE	84h - 1h
SANITIZE - CRYPTO ERASE	84h - 3h

Table 18: Op Codes for NVMe Commands

Codes not listed are reserved. All commands in the table are supported.

Command Name	Op Code (hex)
FLUSH	00h
WRITE	01h
READ	02h
WRITE UNCORRECTABLE	04h
COMPARE	05h
DATASET MANAGEMENT – DEALLOCATE (AD)	09h
DATASET MANAGEMENT – INTEGRAL DATA SET FOR WRITE (IDW)	09h
DATASET MANAGEMENT – INTEGRAL DATA SET FOR READ (IDR)	09h
VERIFY	0Ch

Log Pages

The SSD supports log information as defined in the NVMe specification. Supported information is shown in the following tables:

- Error Information (Log Identifier 01h)
- SMART/Health Information (Log Identifier 02h)
- Firmware Slot Information (Log Identifier 03h)
- Commands Supported and Effects (Log Identifier 05h)
- Device Self-Test (Log Identifier 06h)
- Telemetry Host-Initiated (Log Identifier 07h)
- Telemetry Controller-Initiated (Log Identifier 08h)
- Persistent Event (Log Identifier 0Dh)
- Sanitize Status (Log Identifier 81h)
- Power Loss Notification (Log Identifier EFh)
- Power State Transition (Log Identifier FFh)

Table 19: SMART/Health Information (Log Identifier 02h)

Bytes	Name	Description
0	Critical warning	Indicates critical warnings for the state of the controller. Each bit corresponds to a critical warning type; multiple bits may be set. If a bit is cleared to 0, the critical warning does not apply. Critical warnings may result in an asynchronous event notification to the host. Bit 0; If set to 1, the available spare space has fallen below the threshold. Bit 1; If set to 1, the temperature has exceeded a critical threshold. Bit 2; If set to 1, the device reliability has been degraded due to significant media-related errors or any internal error that degrades device reliability. Bit 3; If set to 1, the media has been placed in read-only mode. Bits 7:4; Reserved
2:1	Temperature	Contains the temperature of the overall device (controller and NVM included) in units of Kelvin. If it exceeds the temperature threshold, an asynchronous event may be issued to the host.
3	Available spare	Contains a normalized percentage (0-100%) of the remaining available spare capacity.
4	Available spare threshold	When the available spare falls below the threshold indicated in this field, an asynchronous event may be issued to the host. The value is indicated as a normalized percentage (0-100%).
5	Percentage used	Contains an estimate of the percentage of the device life used based on the actual device usage and prediction of device life. A value of 100 indicates that the estimated endurance of the device has been consumed, but may not indicate a device failure. The value is allowed to exceed 100. Percentages greater than 254 shall be represented as 255. This value shall be updated once per power-on hour (when the controller is not in a sleep state).
31:6	Reserved	Reserved

Table 19: SMART/Health Information (Log Identifier 02h) (Continued)

Bytes	Name	Description
47:32	Data units read	Contains the number of 512 byte data units the host has read from the controller; this value does not include metadata. This value is reported in thousands (that is, a value of 1 corresponds to 1000 units of 512 bytes read) and is rounded up. For the NVM command set, logical blocks read as part of COMPARE and READ operations shall be included in this value.
63:48	Data units written	Contains the number of 512 byte data units the host has written to the controller; this value does not include metadata. This value is reported in thousands (that is, a value of 1 corresponds to 1000 units of 512 bytes written) and is rounded up. For the NVM command set, logical blocks written as part of WRITE operations shall be included in this value.
79:64	Host READ commands	Contains the number of READ commands completed by the controller. For the NVM command set, this is the number of COMPARE and READ commands.
95:80	Host WRITE commands	Contains the number of WRITE commands completed by the controller. For the NVM command set, this is the number of WRITE commands.
111:96	Controller busy time	Contains the amount of time the controller is busy with I/O commands. The controller is busy when there is a command outstanding to an I/O queue (specifically, a command was issued via an I/O submission queue tail doorbell write and the corresponding completion queue entry has not been posted yet to the associated I/O completion queue. This value is reported in minutes.
127:112	Power cycles	Contains the number of power cycles.
143:128	Power on hours	Contains the number of power-on hours. This does not include time that the controller was powered and in a low-power state condition.
159:144	Unsafe shutdowns	Contains the number of unsafe shutdowns. This count is incremented when a shutdown notification (CC.SHN) is not received prior to loss of power.
175:160	Media and data integrity errors	Contains the number of occurrences where the controller detected an unrecovered data integrity error.
191:176	Number of error info log entries	Contains the number of error information log entries over the life of the controller.
195:192	Warning composite temperature time	Contains the amount of time in minutes that the controller is operational and the composite temperature is greater than or equal to the warning composite temperature threshold (WCTEMP) field and less than the critical composite temperature threshold (CCTEMP) field in the Identify controller data structure. If the value of the WCTEMP or CCTEMP field is 0h, then this field is always cleared to 0h regardless of the composite temperature value.
199:196	Critical composite temperature time	Contains the amount of time in minutes that the controller is operational and the composite temperature is greater the critical composite temperature threshold (CCTEMP) field in the Identify controller data structure. If the value of the CCTEMP field is 0h, then this field is always cleared to 0h regardless of the composite temperature value.
201:200	Temperature Sensor 1	Contains the current temperature reported by temperature sensor 1.
215:202	Reserved	Reserved

Table 19: SMART/Health Information (Log Identifier 02h) (Continued)

Bytes	Name	Description
219:216	Thermal Management Temperature 1 transition count	Contains the number of times the controller transitioned to lower power active power states or performed vendor-specific thermal management actions while minimizing the impact on performance in order to attempt to reduce the Composite Temperature because of the host-controlled thermal management feature. This counter shall not wrap after it reaches its maximum value. A value of zero indicates that this transition has never occurred.
223:220	Thermal Management Temperature 2 transition count	Contains the number of times the controller transitioned to lower power active power states or performed vendor-specific thermal management actions regardless of the impact on performance in order to attempt to reduce the Composite Temperature because of the host-controlled thermal management feature. This counter shall not wrap after it reaches its maximum value. A value of zero indicates that this transition has never occurred.
227:224	Total time for Thermal Management Temperature 1	Contains the number of seconds that the controller transitioned to lower power active power states or performed vendor-specific thermal management actions while minimizing the impact on performance in order to attempt to reduce the Composite Temperature because of the host-controlled thermal management feature. This counter shall not wrap after it reaches its maximum value. A value of zero indicates that this transition has never occurred.
231:228	Total time for Thermal Management Temperature 2	Contains the number of seconds that the controller transitioned to lower power active power states or performed vendor-specific thermal management actions regardless of the impact on performance in order to attempt to reduce the Composite Temperature because of the host controlled thermal management feature. This counter shall not wrap after it reaches its maximum value. A value of zero indicates that this transition has never occurred.
511:232	Reserved	Reserved

System Management Bus

SMBus Out-of-Band Temperature Monitoring

The 2450 SSD uses the SMBus interface for monitoring drive temperature out-of-band. Temperature reported through the SMBus interface is equivalent to the temperature reported through NVMe SMART/Health Information (Log Identifier 02h) and is updated at the same rate. Temperature data is available at the address shown in the table below. Temperature data accurate within ±2°C.

Functionality is defined in the System Management Bus (SMBus) Specification Version 3.1 supporting the following:

- Read word protocol
- Packet error checking (PEC)
- Address resolution protocol (ARP)

Table 20: SMBus Out-of-Band Temperature Monitoring

SMBus Feature	Address	Address Offset	Data Size	Data Format	Unit
Temperature monitoring	4Ah	00h	16 bits	unsigned integer	Kelvin

Notes:
1. Temperature only monitored while the drive is in an operational NVMe power state.
2. ALERT# signal is not supported.
3. Address is 7-bit, lowest bit is R/W#, 0100 101x.
4. Nominal input voltage = 1.8V.
5. SMB_SCL supports input frequency of 100–400 KHz.
6. ARP address is not persistent across power cycles.
7. Error conditions returned as FFFFh.
8. Refer to System Management Bus (SMBus) Specification Version 3.1 for implementing pull-up circuitry.

Interface Connectors

Figure 3: Interface Connections – M.2 Type 2280, 2242, and 2230

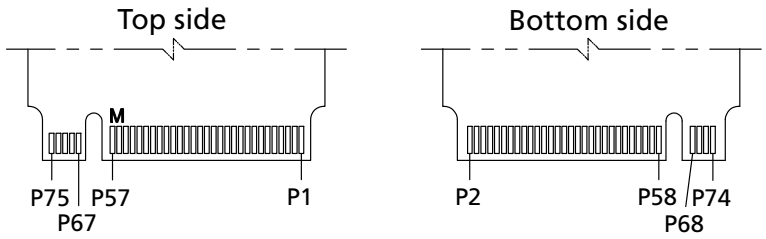


Table 21: Signal Assignments

Top Side			Bottom Side		
Pin #	**Signal Name**	**Description**	**Pin #**	**Signal Name**	**Description**
1	GND	Ground	2	3.3V	+3.3V
3	GND	Ground	4	3.3V	+3.3V
5	PETn3	PCIe TX– Lane 3	6	NC6	No connect
7	PETp3	PCIe TX+ Lane 3	8	PLN#	PLN#
9	GND	Ground	10	DAS	Drive activity signal
11	PERn3	PCIe RX– Lane 3	12	3.3V	+3.3V
13	PERp3	PCIe RX+ Lane 3	14	3.3V	+3.3V
15	GND	Ground	16	3.3V	+3.3V
17	PETn2	PCIe TX– Lane 2	18	3.3V	+3.3V
19	PETp2	PCIe TX+ Lane 2	20	NC20	No connect
21	GND	Ground	22	NC22	No connect
23	PERn2	PCIe RX– Lane 2	24	NC24	No connect
25	PERp2	PCIe RX+ Lane 2	26	NC26	No connect
27	GND	Ground	28	NC28	No connect
29	PETn1	PCIe TX– Lane 1	30	PLA#	Reserved
31	PETp1	PCIe TX+ Lane 1	32	NC32	No connect
33	GND	Ground	34	NC34	No connect
35	PERn1	PCIe RX– Lane 1	36	NC36	No connect
37	PERp1	PCIe RX+ Lane 1	38	NC38	No connect
39	GND	Ground	40	SMB_CLK	SMB_CLK
41	PETn0	PCIe TX– Lane 0	42	SMB_DATA	SMB_DATA
43	PETp0	PCIe TX+ Lane 0	44	ALERT#	ALERT#
45	GND	Ground	46	NC46	No connect
47	PERn0	PCIe RX– Lane 0	48	NC48	No connect
49	PERp0	PCIe RX+ Lane 0	50	PERST#	PERST#
51	GND	Ground	52	CLKREQ#	CLKREQ#

Table 21: Signal Assignments (Continued)

Top Side			Bottom Side		
Pin #	**Signal Name**	**Description**	**Pin #**	**Signal Name**	**Description**
53	REFCLKn	PCIe REFCLK–	54	PEWAKE#	No connect
55	REFCLKp	PCIe REFCLK+	56	MFG_DATA	Reserved
57	GND	Ground	58	MFG_CLOCK	Reserved
Mechanical M Key			**Mechanical M Key**		
67	NC67	No Connect	68	SUSCLK	No connect
69	PEDET	No Connect	70	3.3V	+3.3V
71	GND	Ground	72	3.3V	+3.3V
73	GND	Ground	74	3.3V	+3.3V
75	GND	Ground	–	–	–

Note: 1. DAS behavior defined per the Serial ATA Specification.

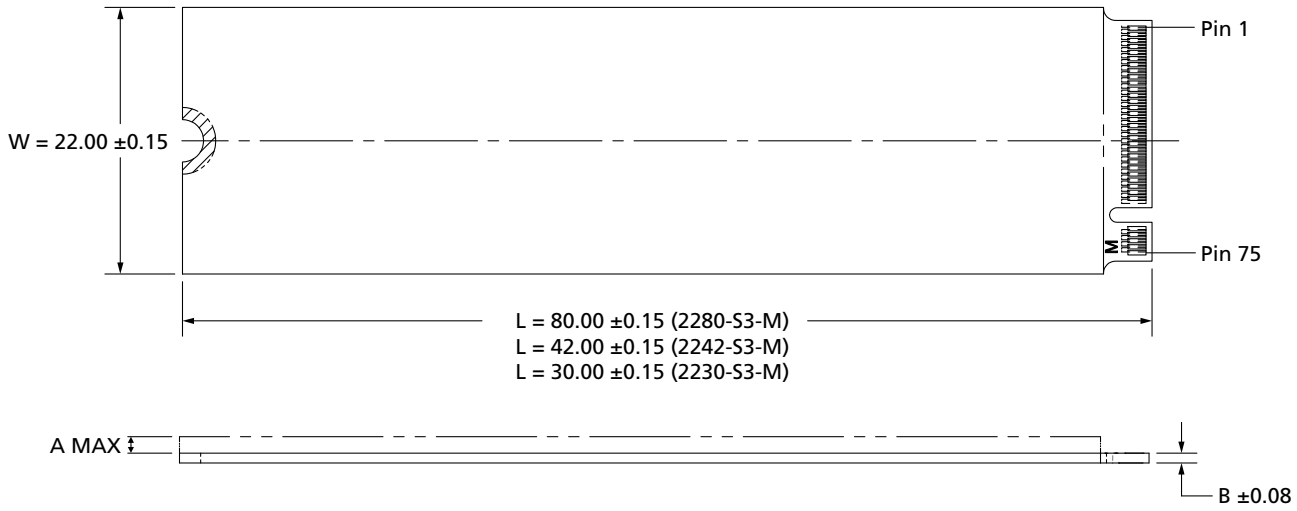
Physical Configuration

M.2 Type 2280, 2242, and 2230

Product mass: 10 grams MAX

Physical dimensions conform to the applicable form factor specifications as listed in the figure below.

Figure 4: M.2 Type 2280, 2242, and 2230 Form Factors



Note: 1. All dimensions are in millimeters.

Table 22: M.2 Type 2280, 2242, and 2230 Form Factor Dimensions

Capacity (GB)	Type	W	L	A	B	Unit
256	2280-S3-M	22	80	1.5	0.8	mm
512						
1024						
256	2242-S3-M		42			
512						
1024						
256	2230-S3-M		30			
512						
1024						

Note: 1. Dimension values per PCI Express M.2 Electromechanical Specification, Revision 1.1.

Compliance

The SSDs comply with the following:

- Micron Green Standard
- CE (Europe): EN55032, EN55024 Class B, RoHS
- UKCA (UK): EN 55032, EN 55024, Class B, RoHS
- Built with sulfur-resistant resistors
- FCC: CFR Title 47, Part 15, Class B
- UL/cUL: approval to UL/IEC 60950 and UL/IEC 62368
- BSMI (Taiwan): approval to CNS 13438 Class B, CNS15663
- RCM (Australia, New Zealand): AS/NZS CISPR32 Class B
- KC RRL (Korea): approval to KN32 Class B, KN 35 Class B

  B 급 기기 (가정용 정보통신기기) 이 기기는 가정용으로 전자파적합등록을한 기기로서 주거 지역에서는 물론 모든지역에서 사용할 수 있습니다.

- W.E.E.E.: Compliance with EU WEEE directive 2012/19/EC. Additional obligations may apply to customers who place these products in the markets where WEEE is enforced.
- TUV (Germany): approval to IEC/EN 60950 and IEC/EN 62368
- V_{CCI} (Japan): 2015-04 Class B

  この装置は、クラス B 情報技術装置です。この装置は、家庭環境で使用することを目的としていますが、この装置がラジオやテレビジョン受信機に近接して使用されると、受信障害を引き起こすことがあります。
  取扱説明書に従って正しい取り扱いをして下さい。
  VCCI－B
- IC (Canada): ICES-003 Class B
  - This Class B digital apparatus complies with Canadian ICES-003.
  - Cet appareil numérique de la classe B est conforme à la norme NMB-003 du Canada.
- Morocco: EN55032, EN55024 Class B
- UkrSEPRO (Ukraine): EN55032 Class B, IEC60950/EN60950, RoHS (Resolution 2017 No. 139)

FCC Rules

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

References

- NVM Express, Revision 1.4
- PCI Express Base Specification, Revision 4.0, Version 1.0
- PCI Express M.2 Electromechanical Specification, Revision 1.1
- TCG Storage Architecture Core Specification Version 2.01 Revision 1.00
- TCG Storage Security Subsystem Class: Opal Specification Version 2.01 Revision 1.00
- TCG Storage Security Subsystem Class: Pyrite Specification Version 2.01 Revision 1.00
- TCG Storage Interface Interactions Specification Version 1.08 Revision 1.06
- TCG Storage Opal SSC Feature Set: PSID Specification Version 1.00 Revision 1.00
- TCG Storage Feature Set: Block SID Authentication Specification Version 1.00 Revision 1.00
- TCG Storage Protection Mechanisms for Secrets Specification Version 1.00 Revision 1.00
- TCG Storage Opal SSC Feature Set: Additional DataStore Tables Version 1.00 Revision 1.00
- Serial ATA Specification
- System Management Bus (SMBus) Specification Version 3.1
- PLI_1.8V_USB_Higher Power ECN
- IDEMA Standard LBA 1-03
- Telcordia Reliability Prediction Procedure for Electronic Equipment SR-332

Revision History

Rev. A – 02/2021

- Initial release

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This data sheet contains initial characterization limits that are subject to change upon full characterization of production devices.